HOT CHIPS 24

Tutorial Day
Monday, August 27, 2012

9:30 am	**Tutorial 1**	**(The Evolution of) Mobile SoC Programming**
9:00 am - 10:40	Mobile SOCs: Connecting Hardware to Apps	Neil Trevett from Khronos
10:40 – 11:10	**BREAK**	
11:10 – 11:25	Camera and Video	Sean Mao, **ArcSoft**
11:25 – 11:40	Vision and Gesture Processing	Itay Katz, **Eyesight**
11:40 – 11:55	Augmented Reality	Ben Blachnitzky, **Metaio**
11:55 – 12:10	Sensor Fusion	Jim Steele**, Sensor Platforms**
12:10 – 12:25	3D Gaming	Daniel Wexler**, the11ers**
12:25 – 1:00 pm	**Panel**	
1:00 – 2:00pm	**Lunch**	
2:00 pm	**Tutorial 2**	**Die Stacking**
2:00 – 2:15	Introduction	Liam Madden, **Xilinx**
2:15 – 2:40	Foundry TSV Enablement For 2.5D/3D Chip Stacking	Remi Yu, **UMC**
2:40 – 3:05	Full Processing Interposer Process	Choon Lee, **Amkor**
3:05 – 3:30	Roadmap for Design and EDA Infrastructure for 3D Products	Riko Radojcic, **Qualcomm**
3:30 – 3:55	Xilinx SSI Technology: Concept to Silicon Development Overview	Shankar Lakka, **Xilinx**
3:55 – 4:10	**BREAK**	
4:10 – 4:35	Memory Consideration and Heterogeneous Die	Bryan Black, **AMD**
4:35 – 5:00	Optical Backplanes with 3D Integrated Photonics?	Ephrem Wu, **Xilinx**
5:00 – 5:30	**Panel**	
5:30 – 7:00 pm	**Reception**	

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SOC Programming Tutorial

Hot Chips 2012

Neil Trevett
Khronos President

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Welcome!

- **An exploration of SOC capabilities from the programmer's perspective**
 - How is mobile silicon connecting to mobile software?
- **Mobile ecosystems and the programming APIs they provide**
 - Mobile OS and open standards for SOC acceleration
- **SOC innovation hotspots**
 - Vision and gesture processing, Augmented Reality, Sensor Fusion Photography and Video Processing, 3D Graphics
- **Illustrate the state of the art in mobile programming**
 - *AND* highlight the issues and challenges still be to solved



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Speakers

Session	Speaker	Company	Title
Connecting Mobile SOC Hardware to Apps	Neil Trevett	Khronos	Khronos President and NVIDIA VP of Mobile Content
Break		Break	
Camera and Video	Sean Mao	ArcSoft	VP Marketing, Advanced Imaging Technologies
Vision and Gesture Processing	Itay Katz	Eyesight	Co-Founder & CTO
Augmented Reality	Ben Blachnitzky	Metaio	Director of R&D
Sensor Fusion	Jim Steele	Sensor Platforms	VP Engineering
3D Gaming	Daniel Wexler	the11ers	CXO
Panel Session		All Speakers	

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Khronos Connects Software to Silicon

- **Khronos APIs define processor acceleration capabilities**
 - Graphics, video, audio, compute, vision and sensor processing



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APIs BY the Industry FOR the Industry

- **Khronos APIs define core device acceleration functionality**
 - Low-level "Foundation" functionality needed on every platform
 - Rigorous conformance tests for cross-vendor consistency
- **Khronos standards have strong industry momentum**
 - 100s of man years invested by industry leading experts
 - Shipping on billions of devices and multiple operating systems
- **Khronos is OPEN for any company to join and participate**
 - Standards are truly open – one company, one vote
 - Solid legal and Intellectual Property framework for industry cooperation
 - Khronos membership fees to cover expenses
- **Khronos standards are FREE to use**
 - Members agree to not request royalties

Silicon



Software

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API Standards Evolution

DESKTOP

OpenGL



OpenCL

New API technology first evolves on high-end platforms

MOBILE

OpenSL|ES

OpenMAX



OpenGL|ES

Mobile is the new platform for apps innovation. Mobile APIs unlock hardware and conserve battery life

INTEROP, VISION AND SENSORS

OpenVL

EGL



StreamInput

Apps embrace mobility's unique strengths and need complex, interoperating APIs with rich sensory inputs e.g. Augmented Reality

WEB

HTML







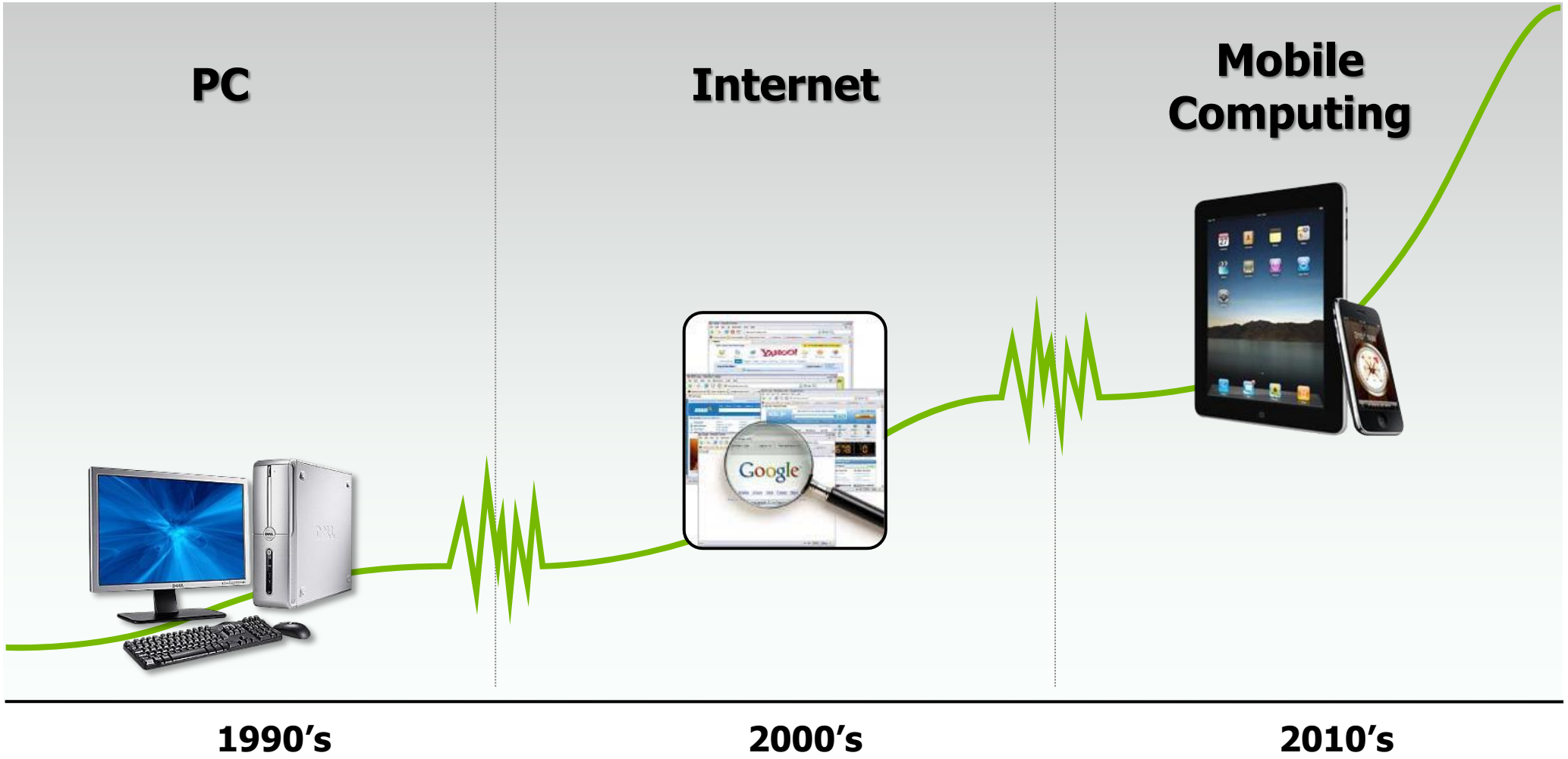
WebGL

WebCL

Diverse platforms – mobile, TV, embedded – means HTML5 will become increasingly important as a universal app platform

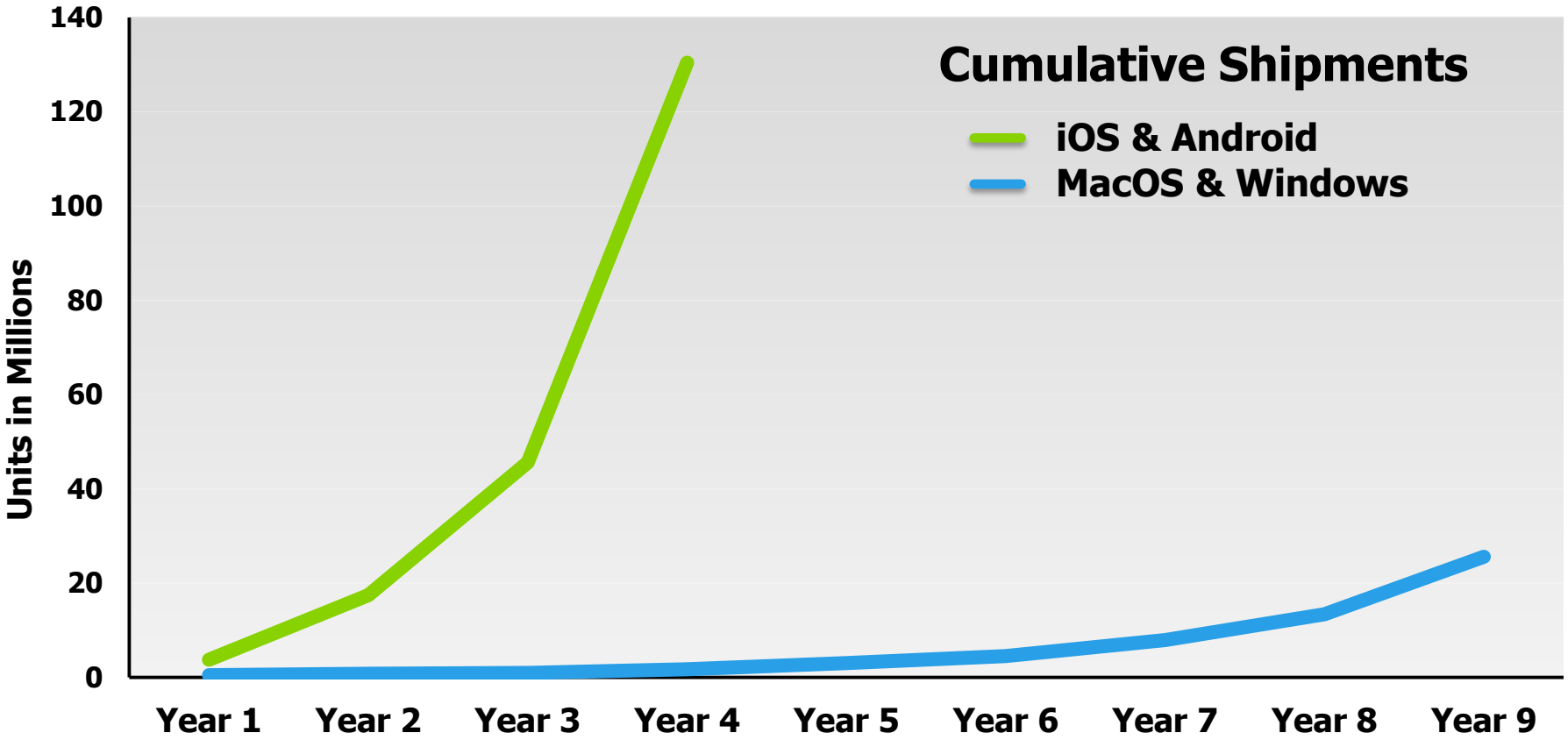
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A New Era in Computing



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20 Years Faster to 100M Per Year

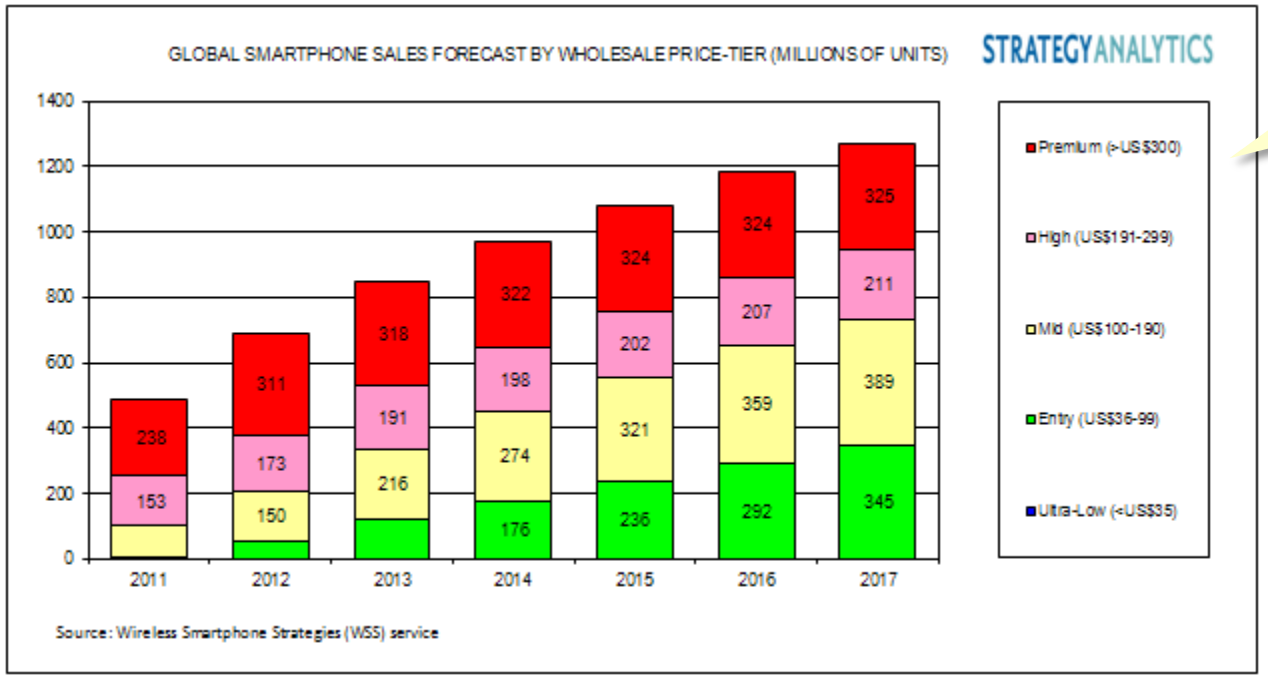


Source: Gartner, Apple, NVIDIA

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The Largest Market Ever

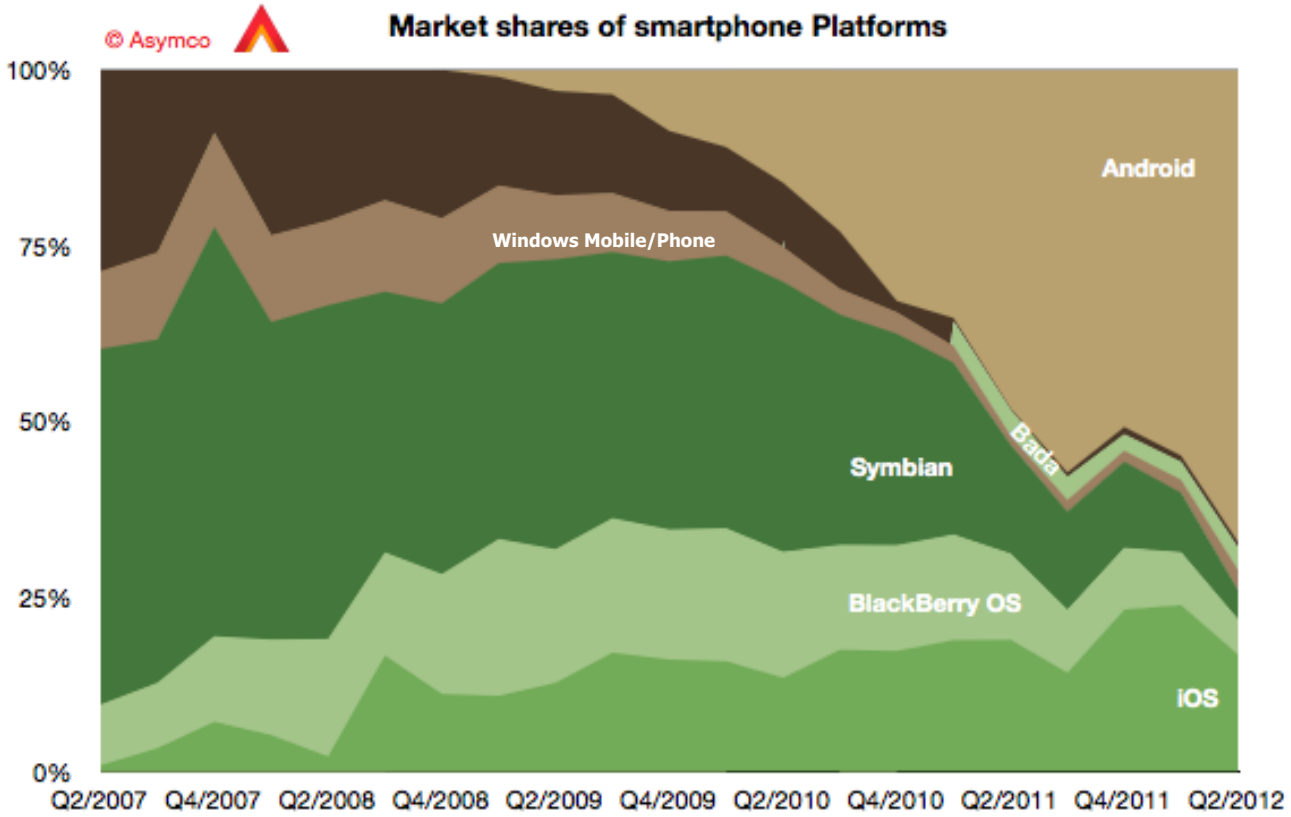
- **IDC - 1.8 billion mobile phones will ship in 2012**
 - By the end of 2016, 2.3 billion mobile phones will ship per year

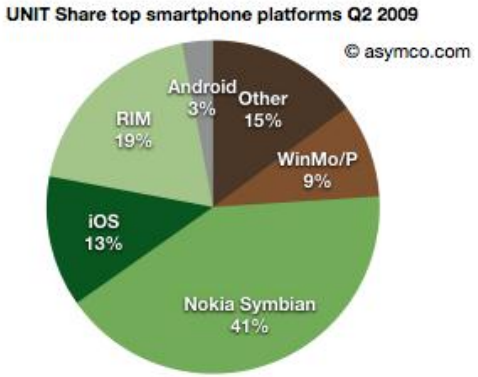


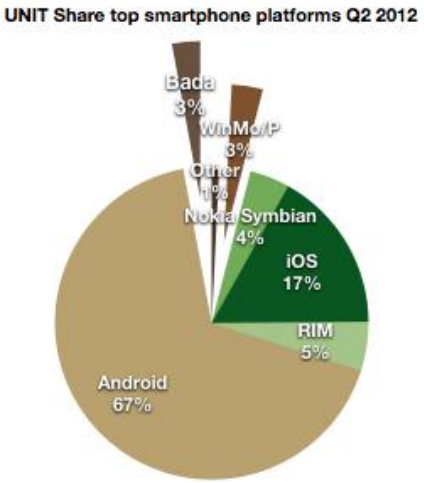
Smart phones accounting for approximately half of total phone market

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Global Smartphone Market Share

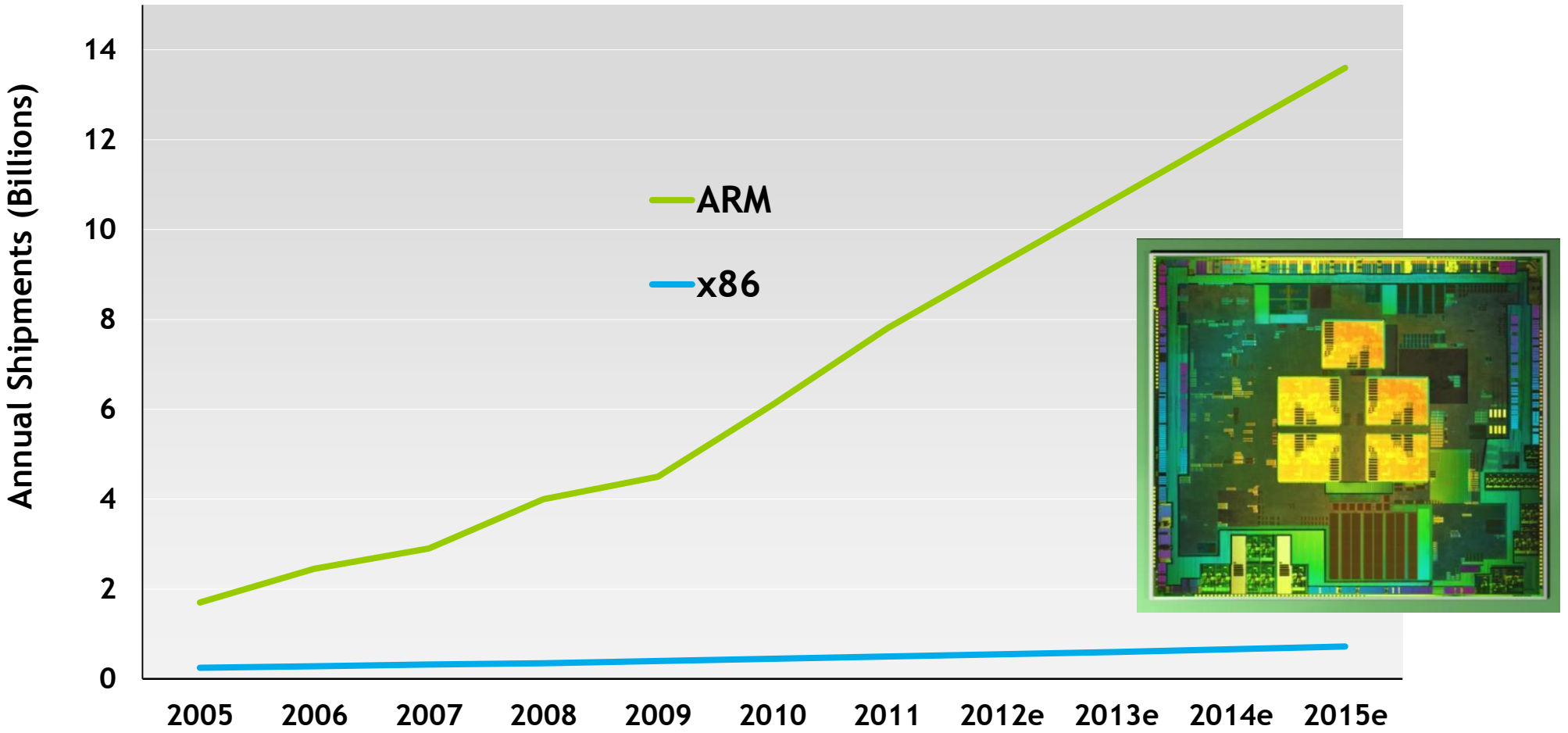






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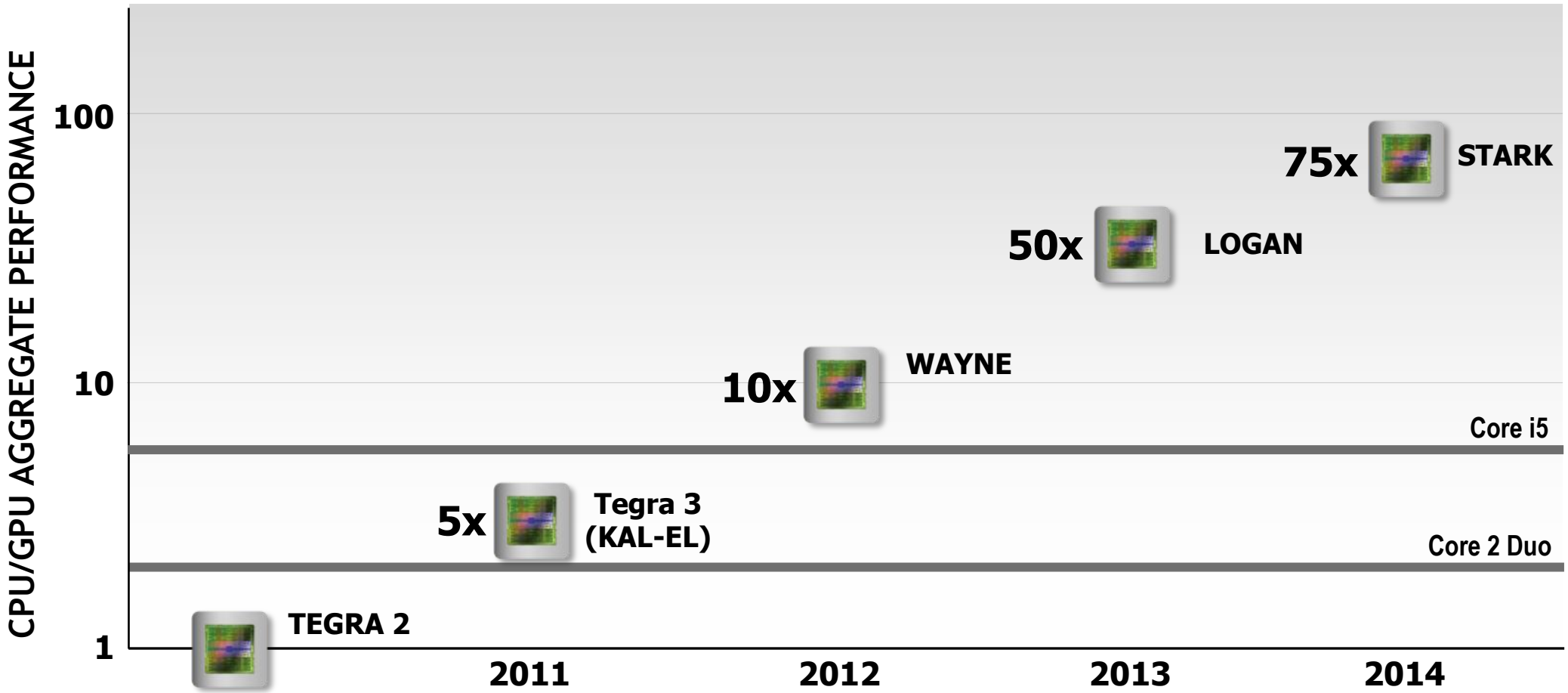
ARM is Licensable and Pervasive



Source: ARM, Mercury Research

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Mobile Performance Increases



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Power is the New Design Limit



- **The Process Fairy keeps bringing more transistors**
 - Transistors are getting cheaper
- **But the Process Fairy isn't helping as much on power as in the past**
 - The End of Voltage Scaling

In the Good Old Days

Leakage was not important, and voltage scaled with feature size

$L' = L/2$
$V' = V/2$
$E' = CV^2 = E/8$
$f' = 2f$
$D' = 1/L^2 = 4D$
$P' = P$

Halve L and get 4x the transistors and 8x the capability for
the same power

The New Reality

Leakage has limited threshold voltage, largely ending voltage scaling

$L' = L/2$
$V' = \sim V$
$E' = CV^2 = E/2$
$f' = \sim 2f$
$D' = 1/L^2 = 4D$
$P' = 4P$

Halve L and get 4x the transistors and 8x the capability for
4x the power!!

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Mobile Thermal Design Point

5” Screen takes 250-500mW



2-4W

7” Screen takes 1W



4-7W

10” Screen takes 1-2W
Resolution makes a difference!
The iPad3 screen takes up to 8W



6-10W



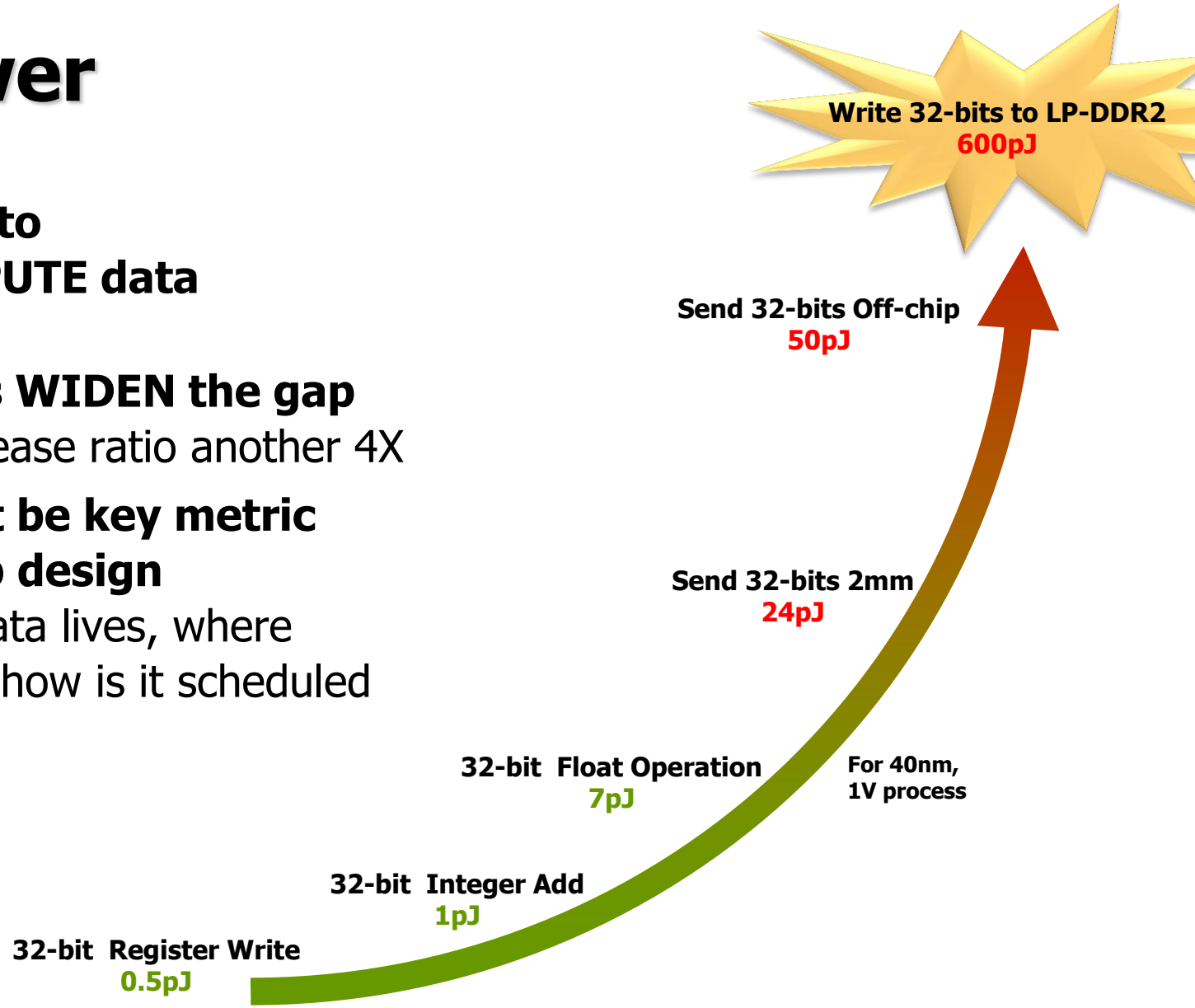
30-90W

Max power the system can use and not break down
Even as battery technology improves - these thermal limits remain

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Apps and Power

- **Much more expensive to MOVE data than COMPUTE data**
- **Process improvements WIDEN the gap**
 - 10nm process will increase ratio another 4X
- **Energy efficiency must be key metric during silicon AND app design**
 - Awareness of where data lives, where computation happens, how is it scheduled



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Energy Optimization Opportunities

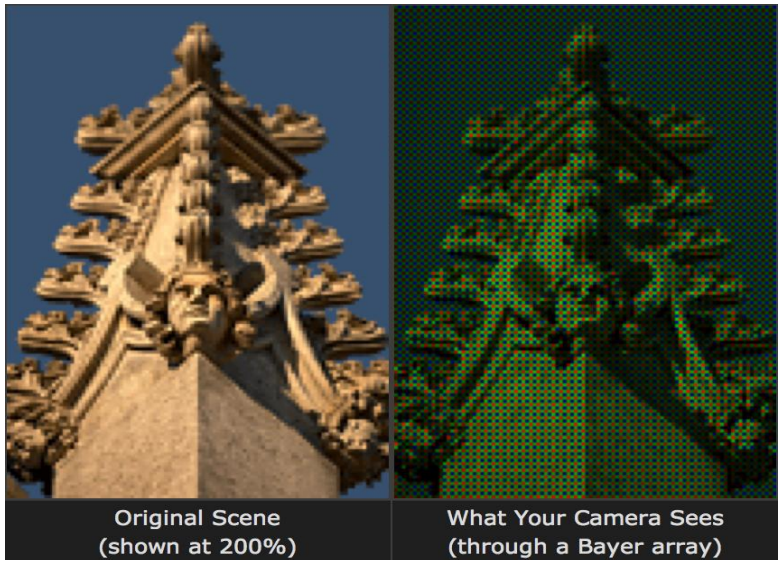
- **Dark Silicon**
 - Lots of space for transistors – just can't turn them all on at same time
 - Multiple specialized hardware units that are only turned on when needed
 - Increase locality and parallelism of computation to save power
- **Dynamic and feedback-driven software power optimization**
 - Instrumentation for energy-aware compilers and profilers
 - Most compilers just look at one thread, take a more global view
 - Power optimizing compiler back-end / installers
- **Smart, holistic use of sensors and peripherals**
 - Motion sensors, cameras, networking, GPS



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Camera Sensor Processing

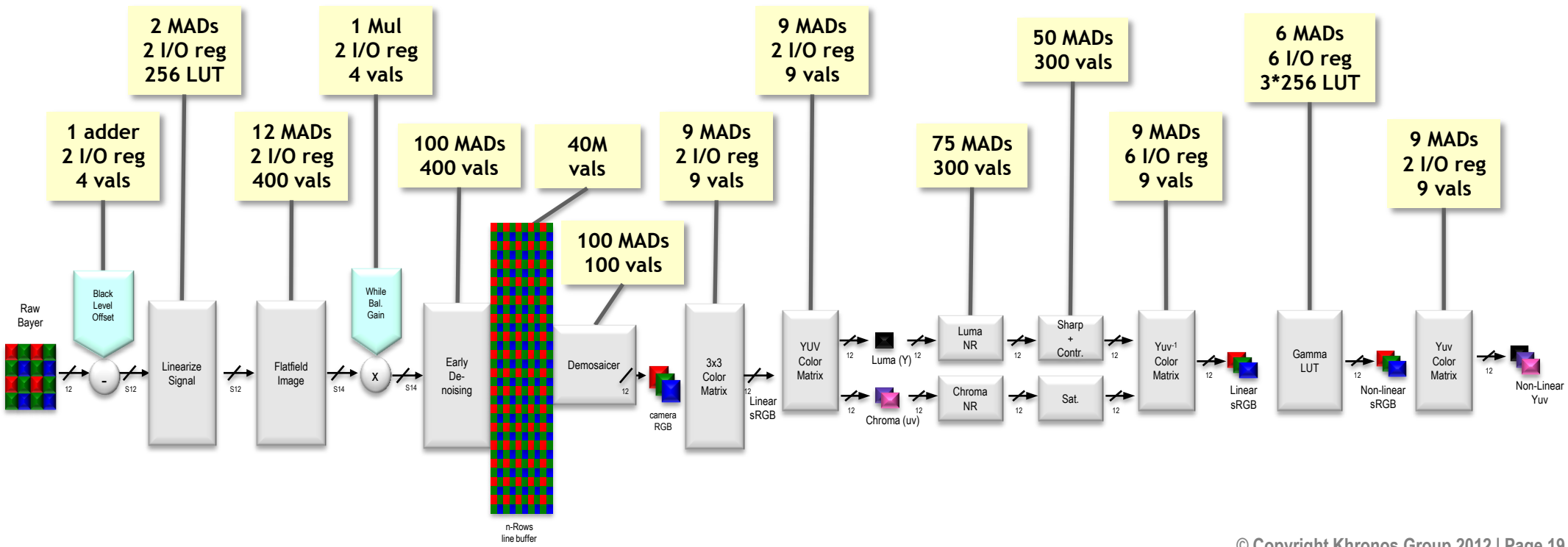
- **CPU**
 - Single processor or Neon SIMD
 - Makes heavy use of general memory
- **GPU**
 - Many way parallelism
 - Efficient image caching into general memory
 - Programmable and flexible
 - Still significant use of cache/memory
- **Camera ISP = Image Signal Processor**
 - Scan-line-based
 - Data flows through compact hardware pipe
 - No global memory used to minimize power
 - Little or no programmability



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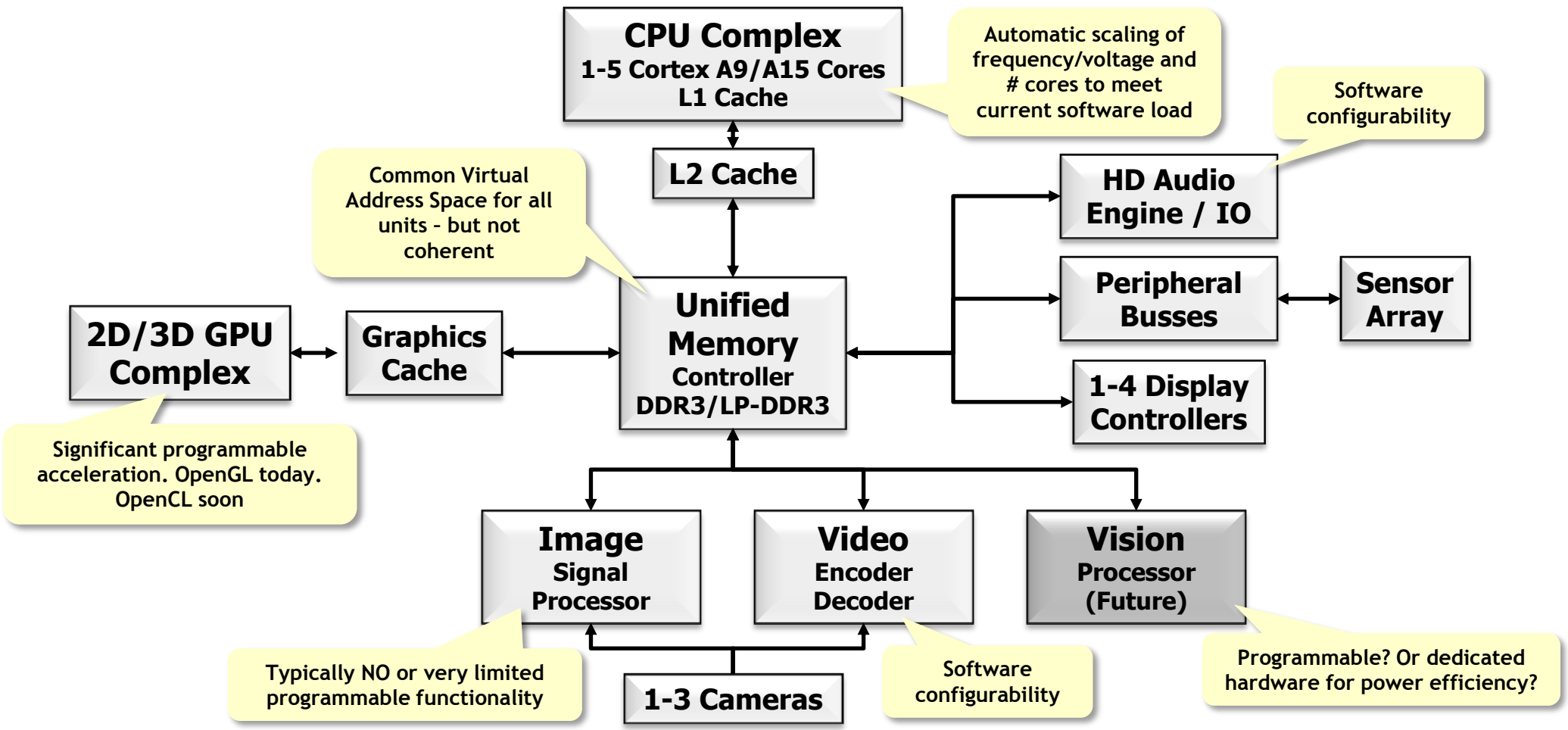
Typical Camera ISP

- ~760 math Ops
- ~42K vals = 670Kb
- 300MHz → ~250Gops



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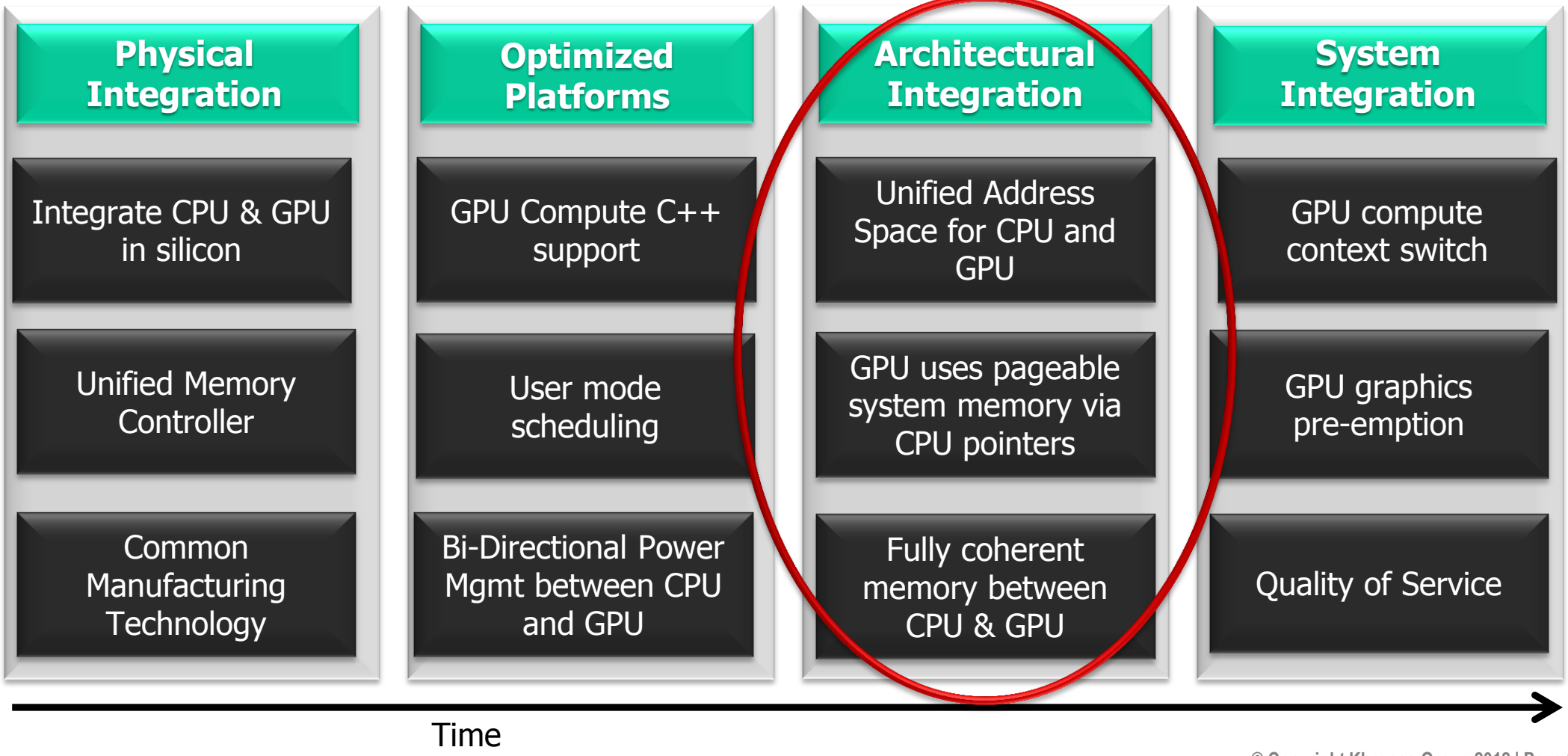
Programmers View of a Typical SOC



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HSA Feature Roadmap

Heterogeneous System Architecture Foundation: AMD, ARM, Imagination, TI, MediaTek



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Mobile Innovation Hot Spots

- **New platform capabilities being driven by SILICON and APIs**



Console-Class 3D

Performance, Quality, Controllers and TV connectivity

OpenGL|ES

Vision - Camera as sensor

Computational Photography
Gesture Processing
Augmented Reality





OpenMAX

- **Media and Image Streaming**
- **Heterogeneous Parallel Processing**

OpenCL



Sensor Fusion

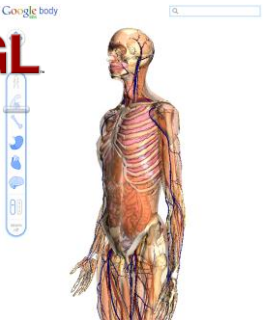
Devices become 'magically' context aware – location, usage, position

StreamInput

WebGL

HTML5

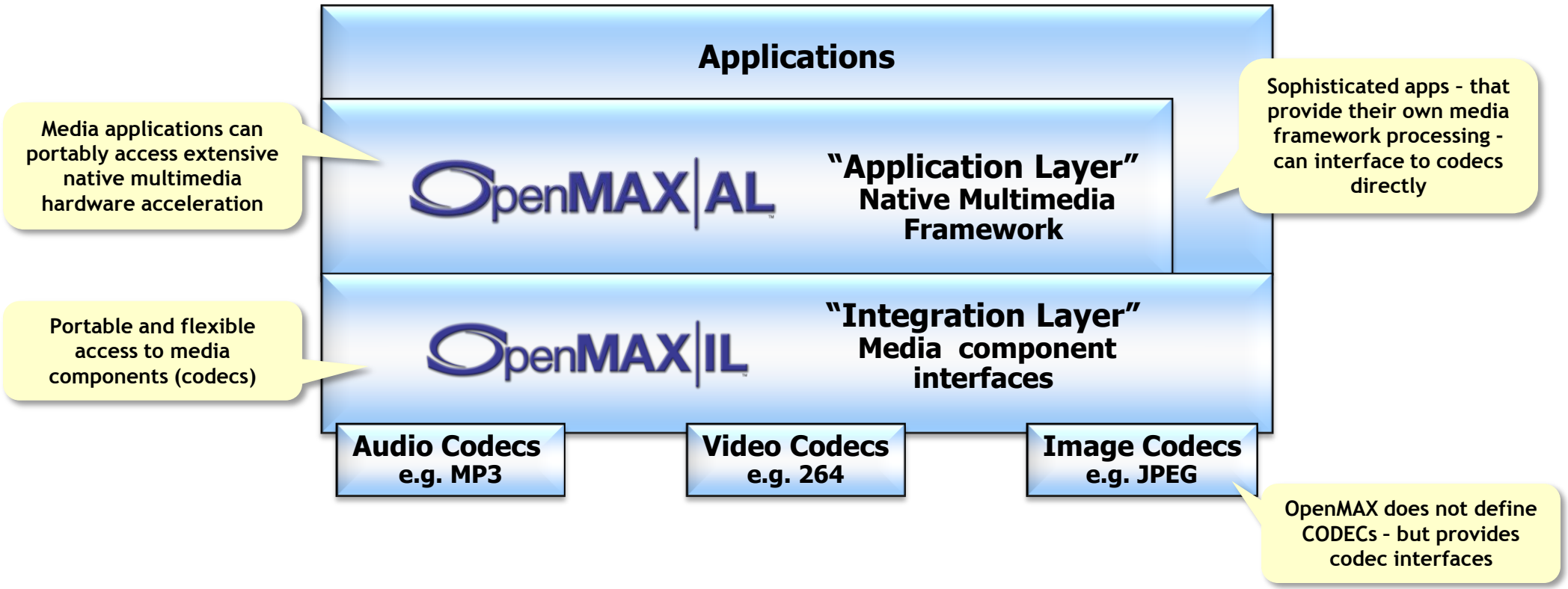
Web Apps that can be discovered on the Net and run on any platform



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OpenMAX - Media Acceleration

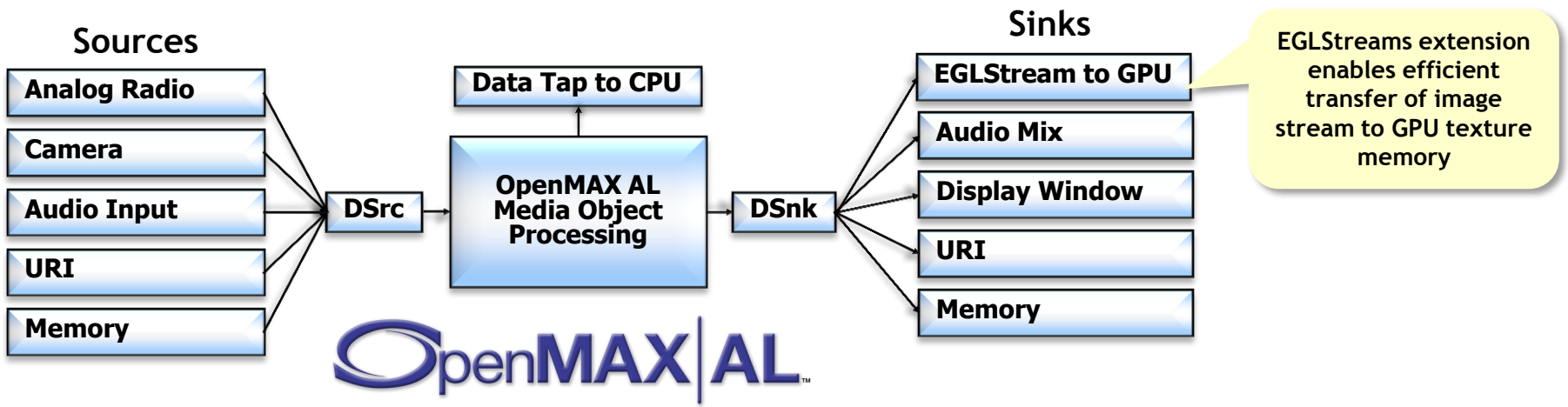
- **Royalty-free , cross-platform open standards**



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OpenMAX AL Streaming Media Framework

- **Enables key video, image stream and camera use cases**
 - Enables optimal hardware acceleration with app portability
- **Create Media Objects to play and process images and video with AV sync**
 - Connect to variety of input and output objects to PLAY and RECORD media
- **Full range of video effects and controls**
 - Including playback rate, post processing, and image manipulation



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Accelerating Streaming Media

DRM Movies

- Inject encrypted elementary streams into decrypt/decode/render
- Dynamic format changes
- Support for Widevine

HD Video Teleconferencing

- Inject video into decode/render
- Extract video from capture/render
- Extended controls (fine-grained codec query/config, force key frames)

Video Editing

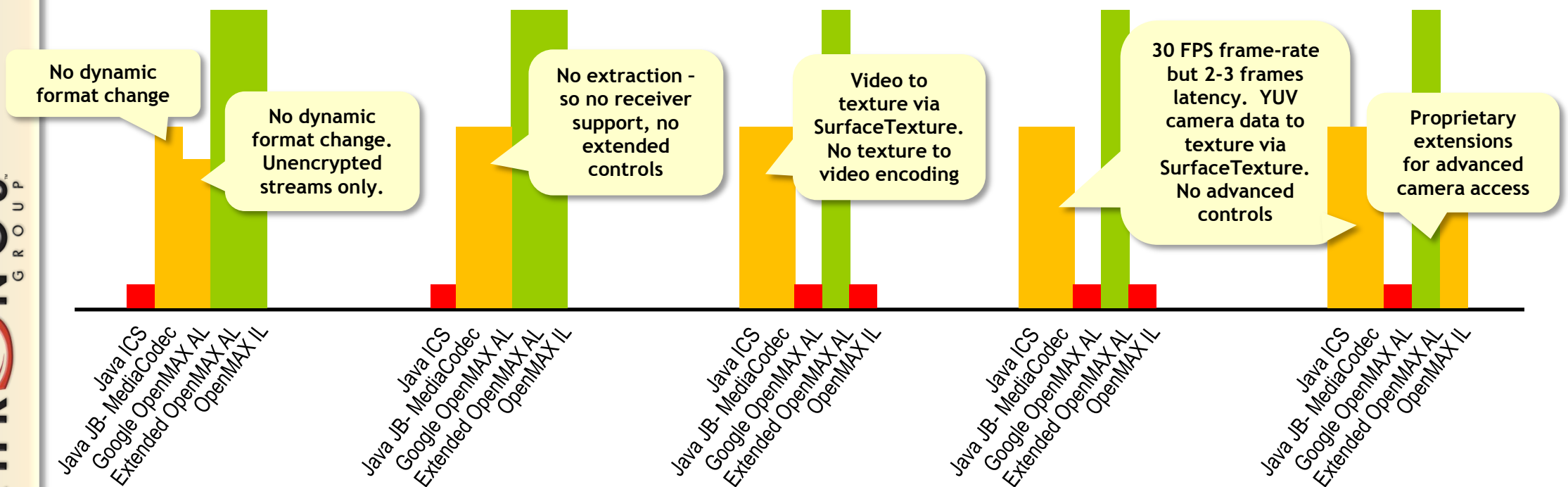
- Video decoding to texture
- Texture to video encoding

Augmented Reality

- High frame-rate, low latency camera capture to app and GPU texture
- Advanced camera control over format, ROI

Computational Photography

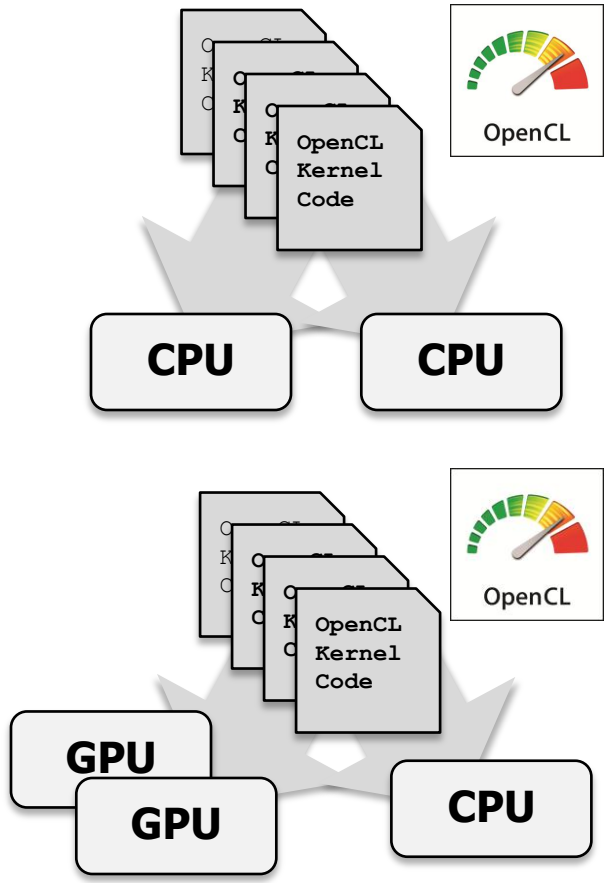
- Fast, low latency camera capture to app and GPU texture
- Advanced camera control over format, bracketed burst mode with sequenced key/value pairs



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OpenCL – Heterogeneous Computing

- **Native framework for programming diverse parallel computing resources**
 - CPU, GPU, DSP – as well as hardware blocks(!)
- **Powerful, low-level flexibility**
 - Foundational access to compute resources for higher-level engines, frameworks and languages
- **Embedded profile**
 - No need for a separate "ES" spec
 - Reduces precision requirements

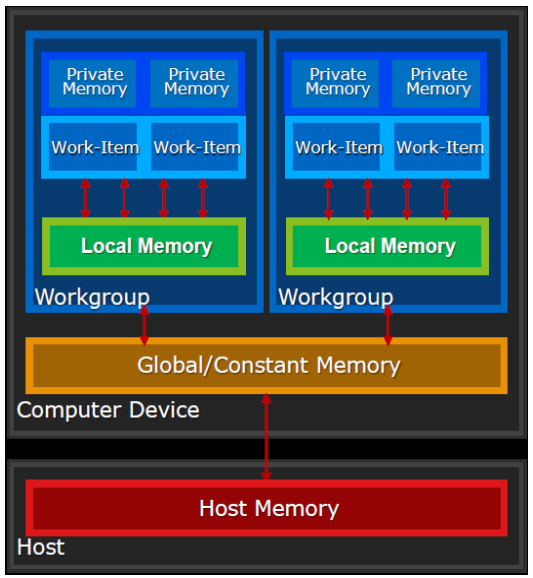


One code tree can be executed on CPUs or GPUs

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OpenCL Overview

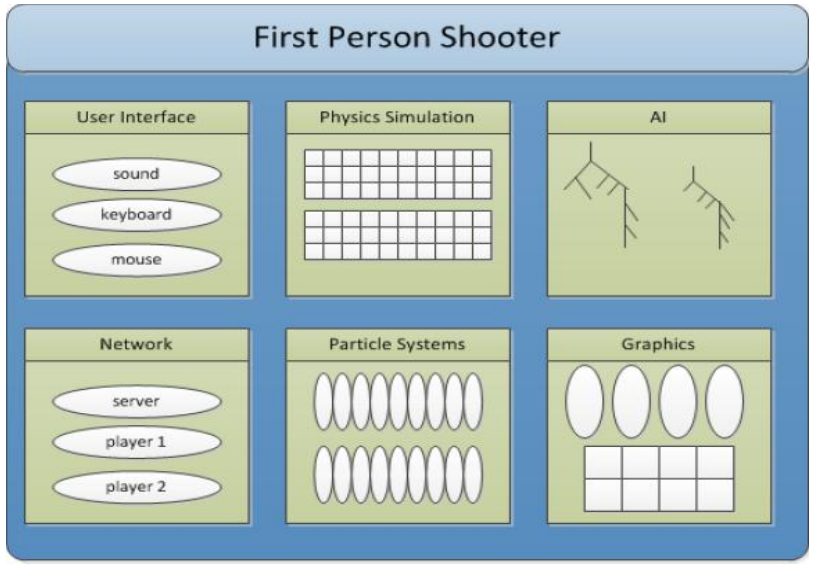
- **C Platform Layer API**
 - Query, select and initialize compute devices
- **Kernel Language Specification**
 - Subset of ISO C99 with language extensions
 - Well-defined numerical accuracy - IEEE 754 rounding with specified max error
 - Rich set of built-in functions: cross, dot, sin, cos, pow, log …
- **C Runtime API**
 - Run-time or build-time compilation of kernels
 - Execute compute kernels across multiple devices
- **Memory management is explicit**
 - Application must move data from host → global → local and back
 - Implementations can optimize data movement in Unified memory systems



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OpenCL: Execution Model

- **Kernel**
 - Basic unit of executable code ~ C function
 - Data-parallel or task-parallel
- **Program**
 - Collection of kernels and functions ~ dynamic library with run-time linking
- **Command Queue**
 - Applications queue kernels & data transfers
 - Performed in-order or out-of-order
- **Work-item**
 - An execution of a kernel by a processing element ~ thread
- **Work-group**
 - A collection of related work-items that execute on a single compute unit ~ core

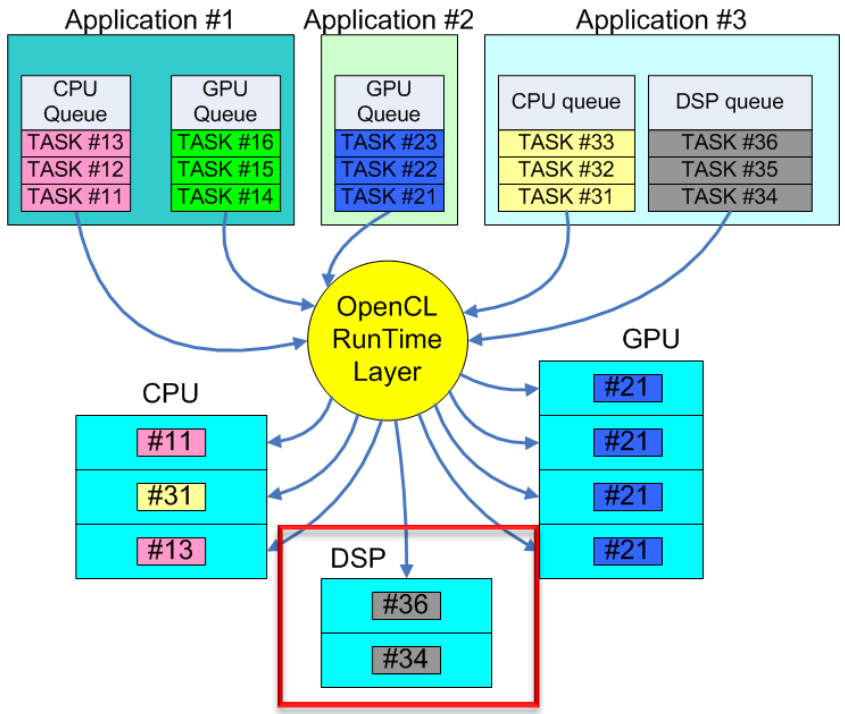


Example of parallelism types

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Custom Devices and Built-in Kernels

- **Embedded platforms often contain specialized hardware and firmware**
 - That cannot support OpenCL C
- **Built-in kernels can represent these hardware and firmware capabilities**
 - Such as video encode/decode, camera ISP
- **Hardware can be integrated and controlled from the OpenCL framework**
 - Can enqueue built-in kernels to custom devices alongside OpenCL kernels
- **OpenCL becomes a powerful coordinating framework for diverse resources**
 - Programmable and non-programmable devices controlled by one run-time

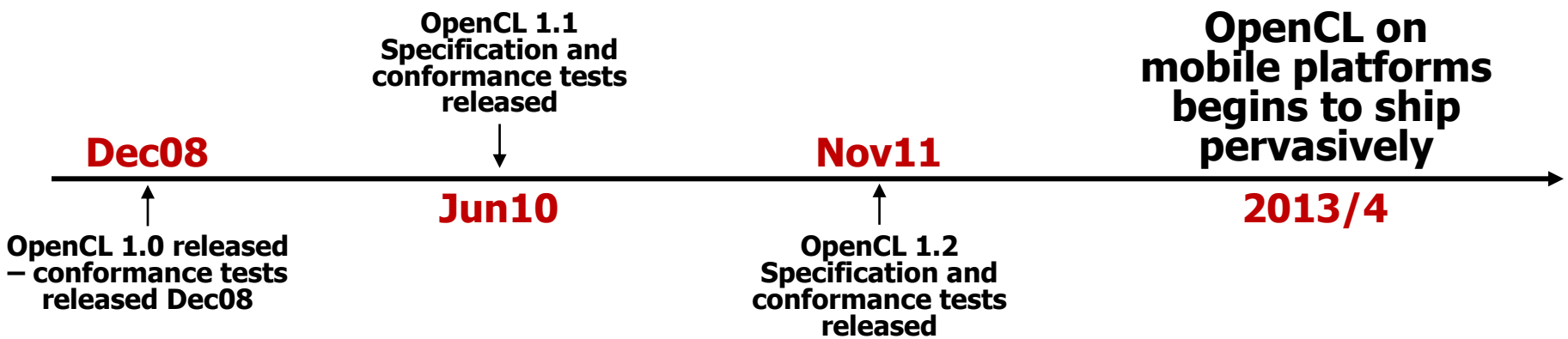


Built-in kernels enable control of specialized processors and hardware from OpenCL run-time

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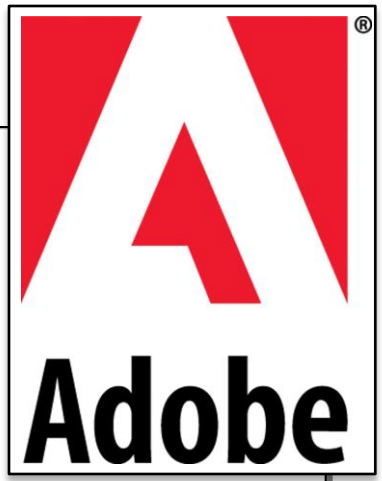
OpenCL Milestones

- **Six months from proposal to released OpenCL 1.0 specification**
 - Due to a strong initial proposal and a shared commercial incentive
- **Multiple conformant implementations shipping on desktop**
 - For CPUs and GPUs on multiple OS
- **18 month cadence between releases**
 - Backwards compatibility protects software investment



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Adobe at SIGGRAPH 2012



Adobe ♥ OpenCL

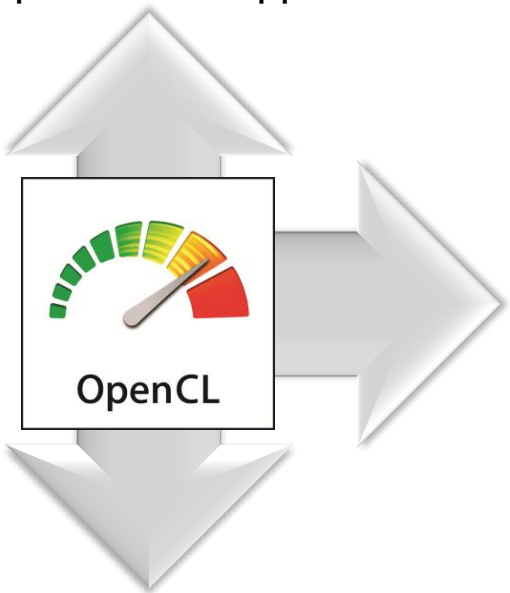
- **Compute API supported across vendors**
- **Programming model familiar to C programmers**
- **Demonstrated performance**
- **Same compute kernels on CPU and GPU!**

- **Adobe is now active member of OpenCL working group**
 - Contributing Adobe's experience and minds to continue OpenCL evolution

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OpenCL Roadmap

OpenCL-HLM (High Level Model)
Exploring high-level programming model, unifying host and device execution environments through language syntax for increased usability and broader optimization opportunities



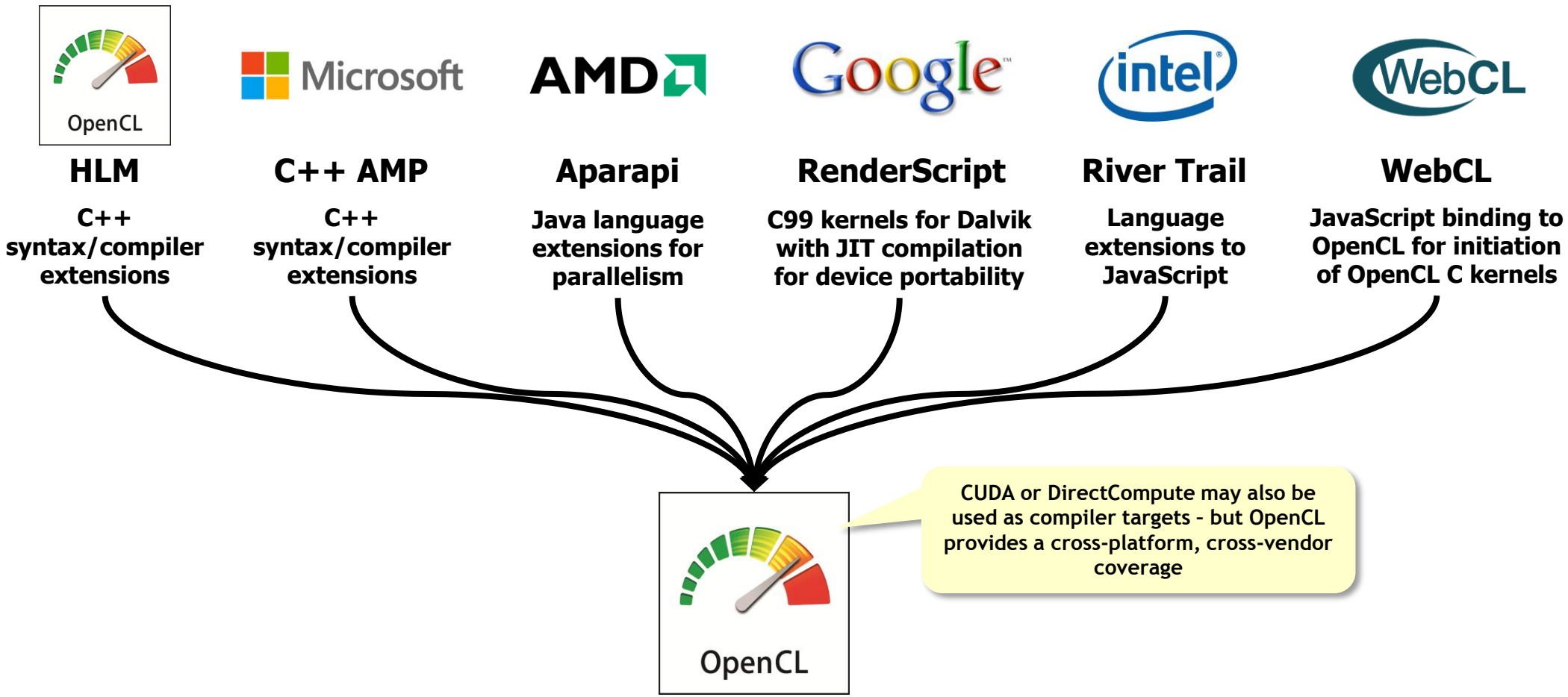
Considering ways to exploit unified and shared virtual memory systems where available

Long-term Core Roadmap
Exploring enhanced memory and execution model flexibility to catalyze and expose emerging hardware capabilities

OpenCL-SPIR (Standard Parallel Intermediate Representation)
Exploring LLVM-based, low-level Intermediate Representation for code obfuscation/security and to provide target back-end for alternative high-level languages

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OpenCL as Parallel Compute Foundation



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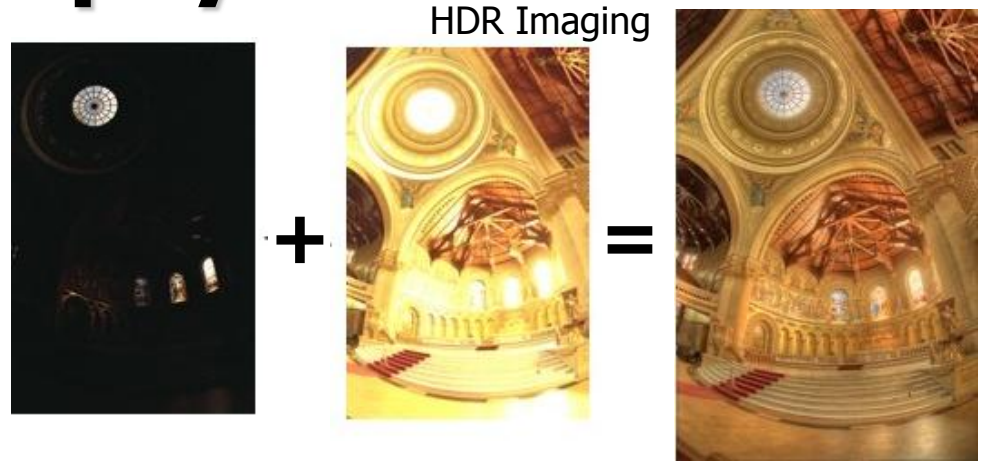
Computational Photography

- **Many advanced photo apps today run on a single CPU**
 - Suboptimal performance and power
- **OpenCL is platform to harness CPUs/GPUs for advanced imaging**
 - Even if code is 'branchy'

"The tablet … has new multimedia capabilities, including a computational camera, which lets devs tap directly into its computational capability through new application programming interfaces such as OpenCL. That access enables next-generation use cases such as light-field cameras for mobile devices."

QUALCOMM

HDR Imaging





Panorama Stitching

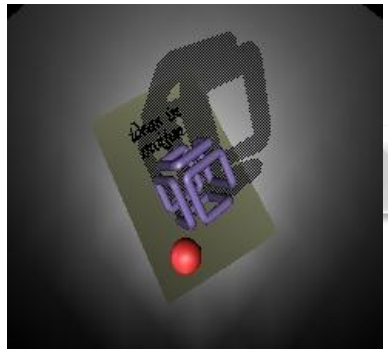


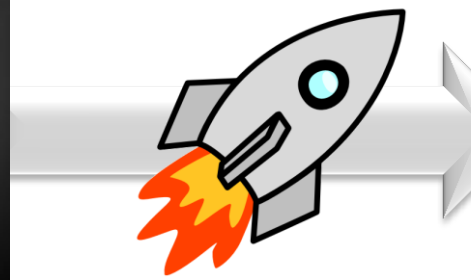
Flash / no-flash imaging

OpenGL 20th Birthday - Then and Now



Ideas in Motion - *SGI*





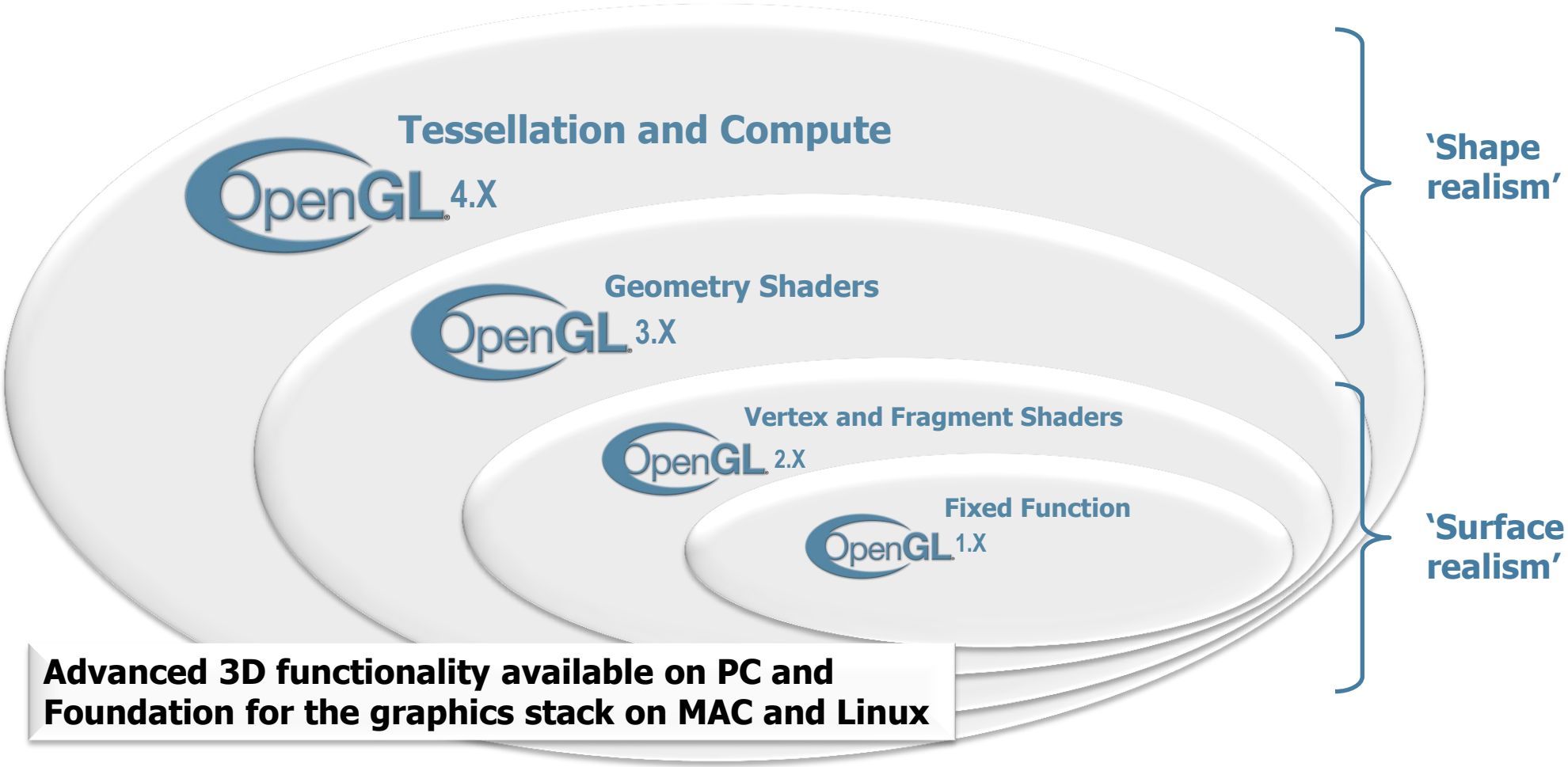
Rage - *id Software*



	1992 Reality Engine 8 Geometry Engines 4 Raster Manager boards	2012 Mobile NVIDIA Tegra 3 Nexus 7 Android Tablet	2012 PC NVIDIA GeForce GTX 680 Kepler GK104
Triangles / sec (millions)	1	103 (x103)	1800 (x1800)
Pixel Fragments / sec (millions)	240	1040 (x4.3)	14,400 (x60)
GigaFLOPS	0.64	15.6 (x25)	3090 (x4830)
	1.5KW	**<5W**	

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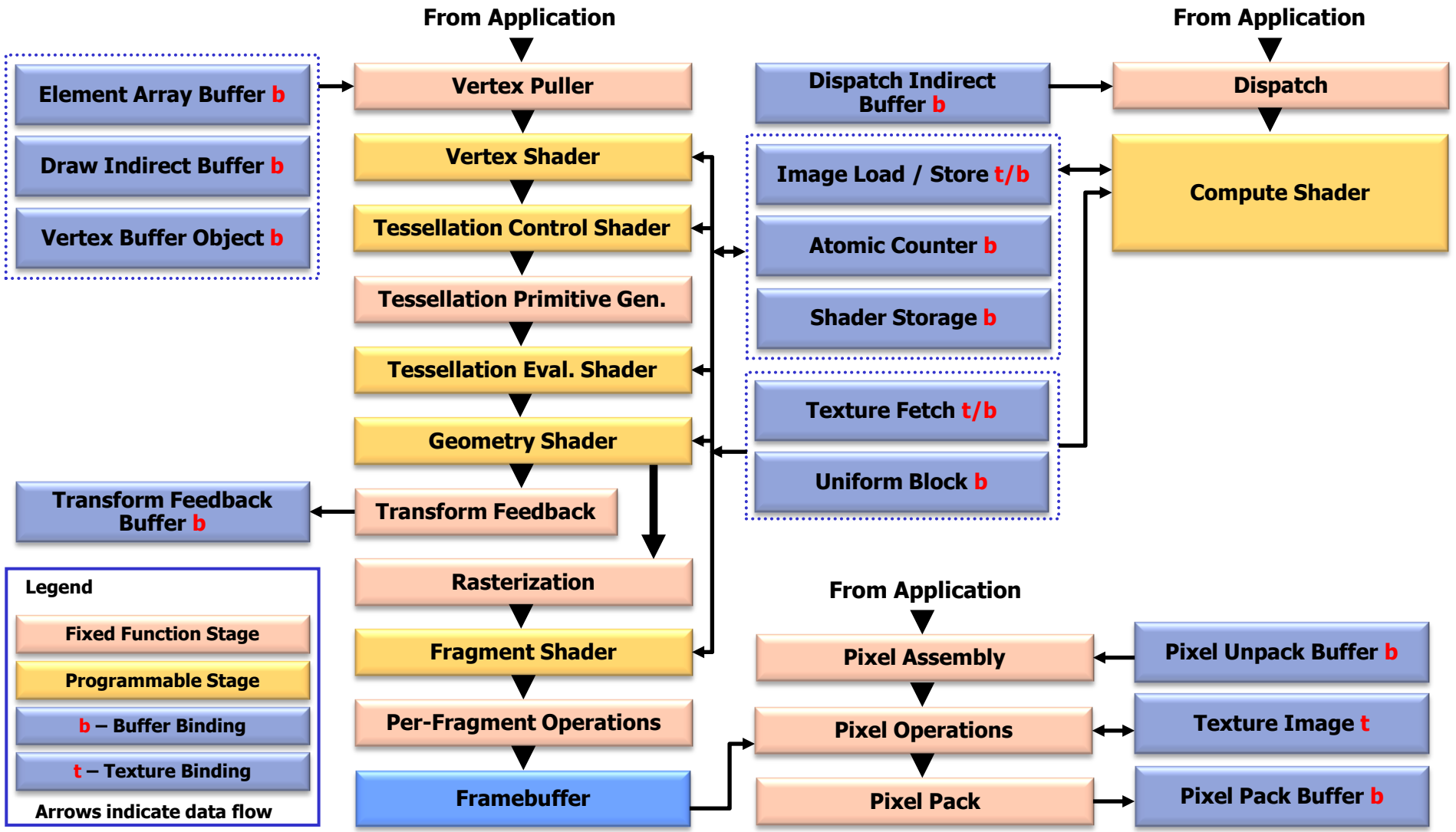
OpenGL for Each Hardware Generation



Advanced 3D functionality available on PC and Foundation for the graphics stack on MAC and Linux

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OpenGL 4.3 with Compute Shaders



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Compute Shaders

- **Execute algorithmically general purpose GLSL shaders**
 - Operate on uniforms, images and textures
- **Process graphics data in the context of the graphics pipeline**
 - Easier than interoperating with a compute API IF processing 'close to the pixel'
- **Complementary to OpenCL**
 - Not a full heterogonous (CPU/GPU) programming framework using full ANSI C
- **Standard part of all OpenGL 4.3 implementations**
 - Matches DirectX 11 functionality



Physics



AI Simulation



Ray Tracing



Imaging

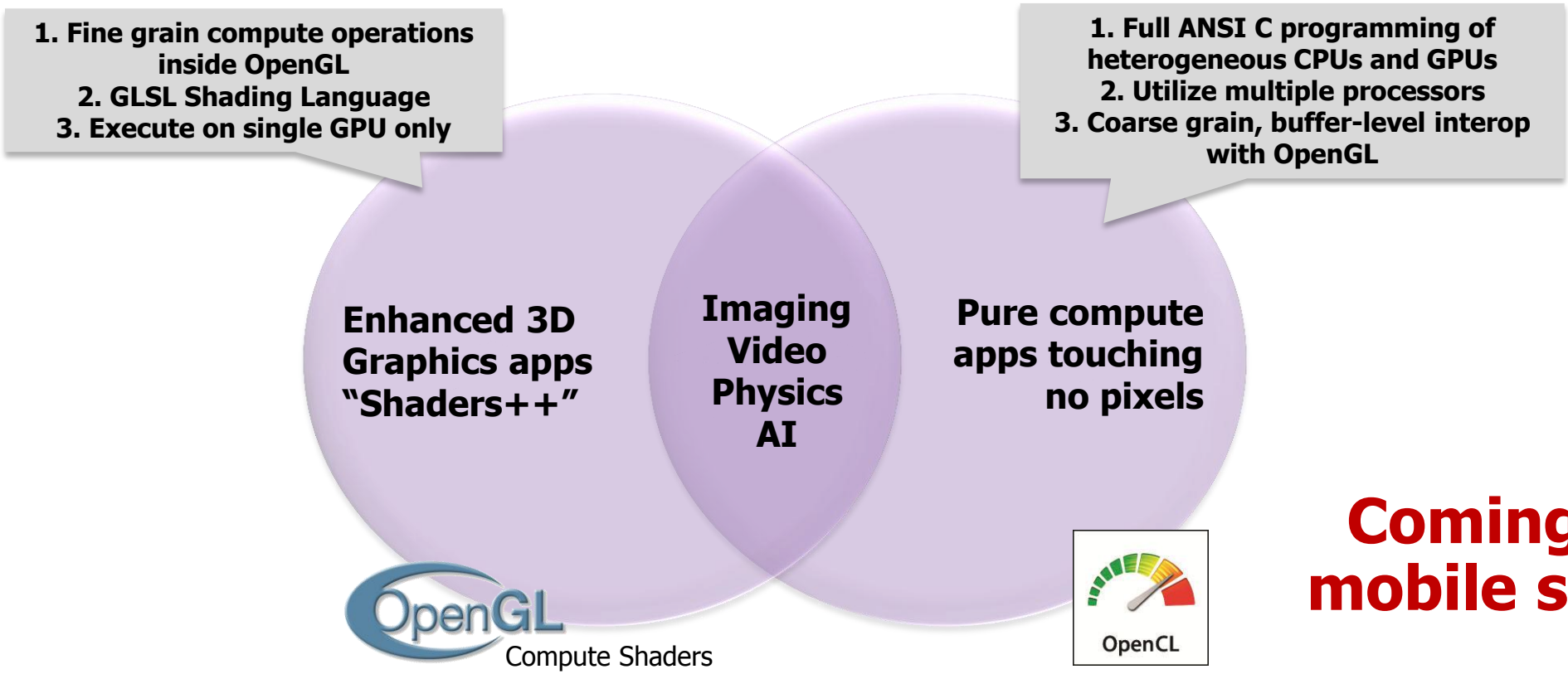


Global Illumination

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OpenCL and OpenGL Compute Shaders

- **OpenGL compute shaders and OpenCL support distinctly different use cases**
 - OpenCL provides a significantly more powerful and complete compute solution



Coming to mobile soon!

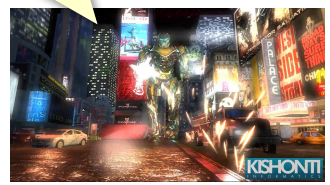
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OpenGL ES

- **Streamlined subset of desktop OpenGL for embedded and mobile devices**







ES3 is backward compatible - so new features can be added incrementally

OpenGL ES 1.1 Content

OpenGL ES 2.0 Content

OpenGL ES 3.0 Content

OpenGL ES 1.1 Platforms Released

OpenGL ES 2.0 Platforms Released

OpenGL ES 3.0 Platforms Released

OpenGL ES 1.0 Spec Released

OpenGL ES 1.1 Spec Released

OpenGL ES 2.0 Spec Released

OpenGL ES 3.0 Spec Released

GL4/DX11-class Capabilities come to ES ??

OpenGL1.5

OpenGL2.0

OpenGL2.1

OpenGL3.1

OpenGL3.0

OpenGL3.2

OpenGL3.3

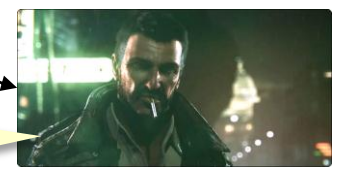
OpenGL4.0

OpenGL4.1

OpenGL4.2

OpenGL 4.3

OpenGL 4.3 is a superset of DX11



2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015

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OpenGL ES 3.0 Highlights

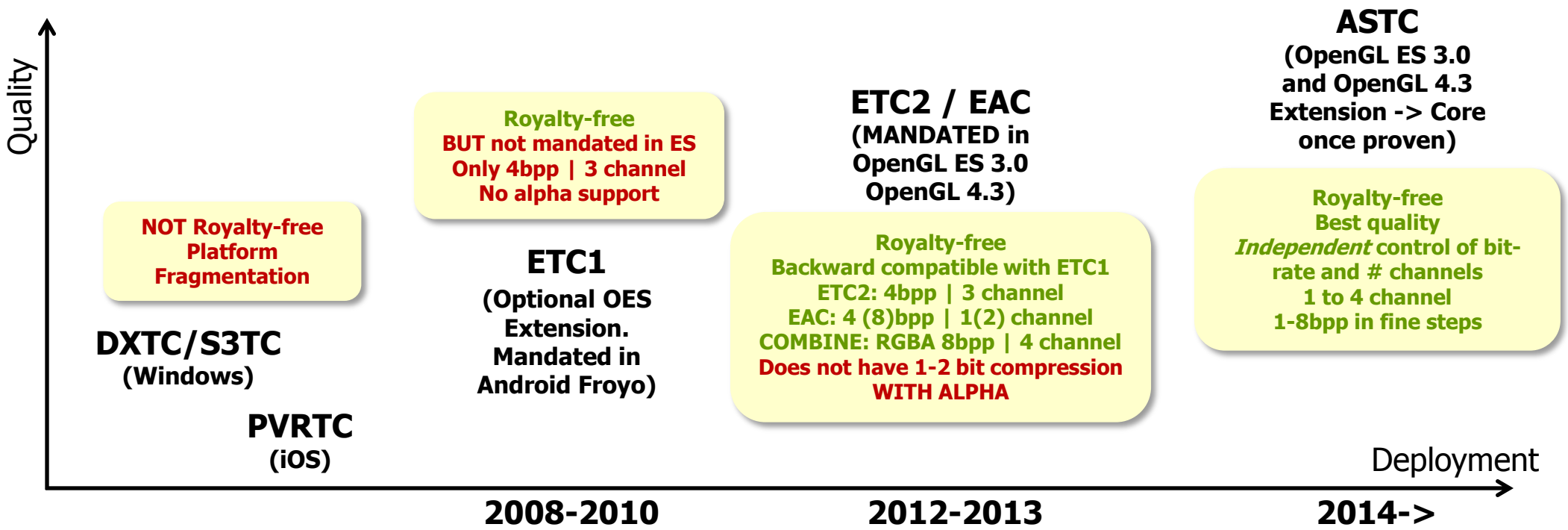
- **Better looking, faster performing games and apps – at lower power**
 - Incorporates proven features from OpenGL 3.3 / 4.x
 - 32-bit integers and floats in shader programs
 - NPOT, 3D textures, depth textures, texture arrays
 - Multiple Render Targets for deferred rendering, Occlusion Queries
 - Instanced Rendering, Transform Feedback …
- **Make life better for the programmer**
 - Tighter requirements for supported features to reduce implementation variability
- **Backward compatible with OpenGL ES 2.0**
 - OpenGL ES 2.0 apps continue to run unmodified
- **Standardized Texture Compression**
 - #1 developer request!



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Texture Compression is Key

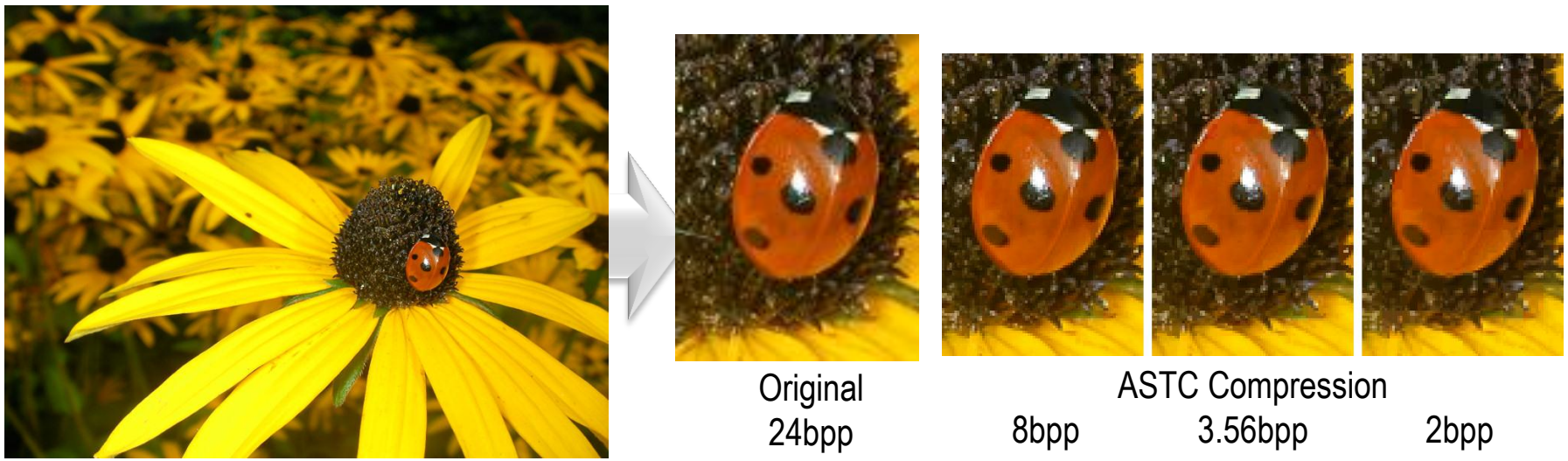
- **Texture compression saves precious resources**
 - Saves network bandwidth, device memory space AND memory bandwidth
- **Developers need the same texture compression EVERYWHERE**
 - Otherwise portable apps – such as WebGL need multiple copies of same texture



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ASTC – Future Universal Texture Standard?

- **Adaptive Scalable Texture Compression (ASTC)**
 - Quality significantly exceeds S3TC or PVRTC at same bit rate
- **Industry-leading orthogonal compression rate and format flexibility**
 - 1 to 4 color components: R / RG / RGB / RGBA
 - Choice of bit rate: from 8bpp to <1bpp in fine steps
- **ASTC is royalty-free and so is available to be universally adopted**
 - Shipping as extension today for industry feedback



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Kishonti GLBenchmark 3.0



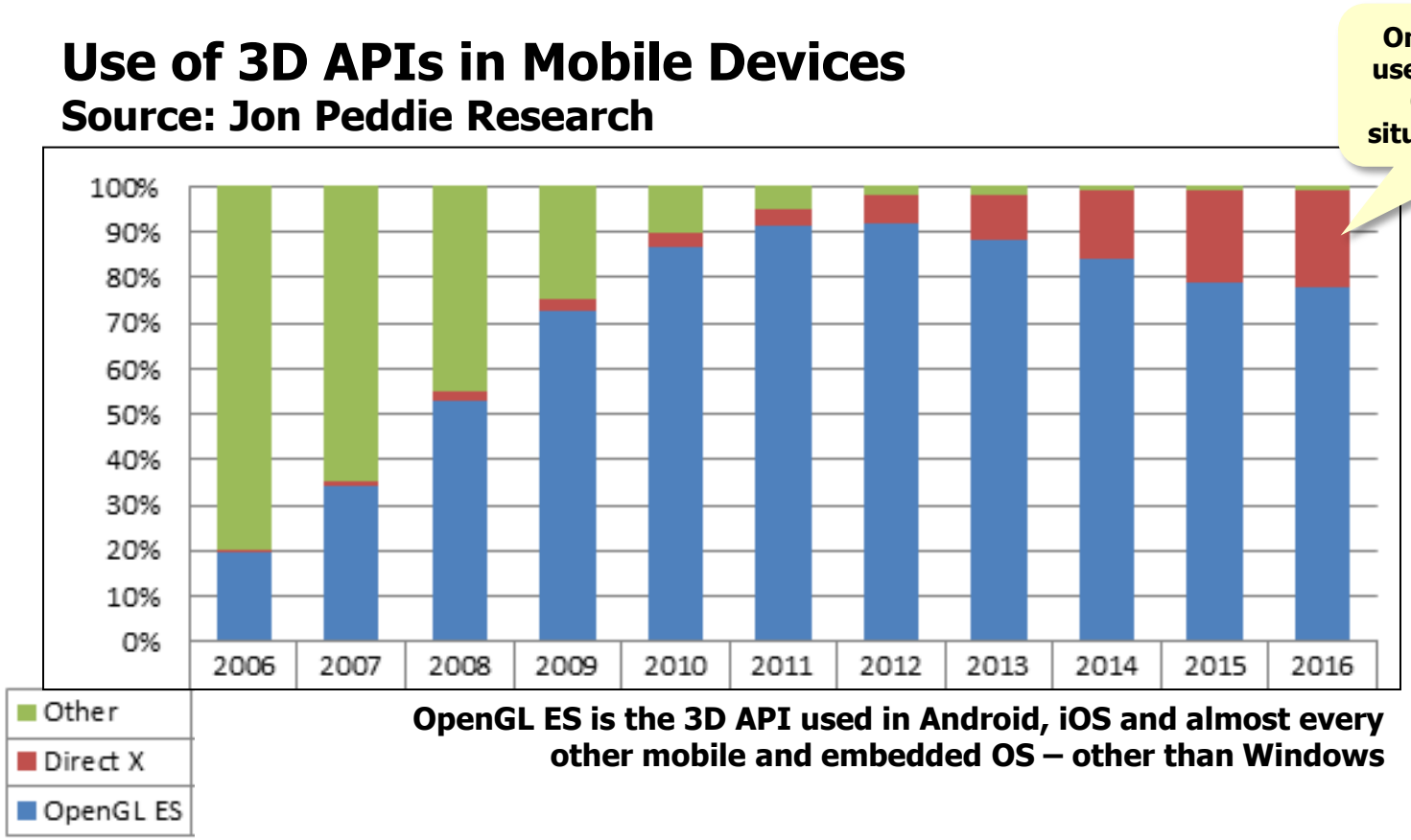
Kishonti "GLBenchmark 3.0" preliminary

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OpenGL ES Deployment in Mobile

Use of 3D APIs in Mobile Devices

Source: Jon Peddie Research



On PC – DirectX is used for most apps. On mobile the situation is reversed





OpenGL ES is the 3D API used in Android, iOS and almost every other mobile and embedded OS – other than Windows

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Visual-based Augmented Reality



Camera video stream sent to the compositor





Camera images used to track the camera's location and orientation

3D augmentations composited with video stream

Camera Tracking

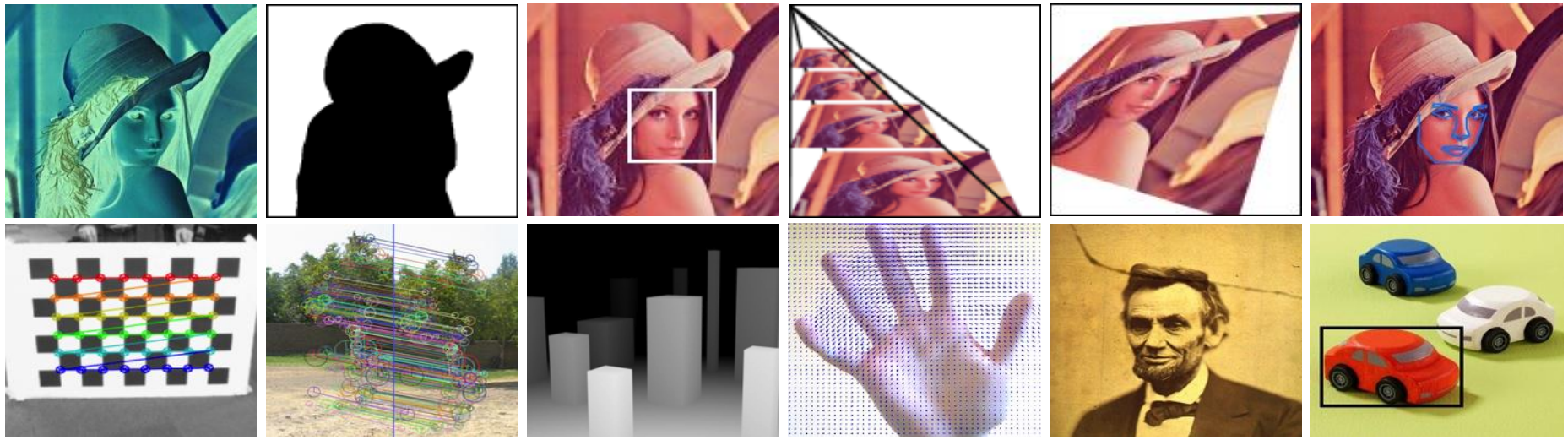
3D Augmentation Rendering

Other on-device Sensors

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OpenCV

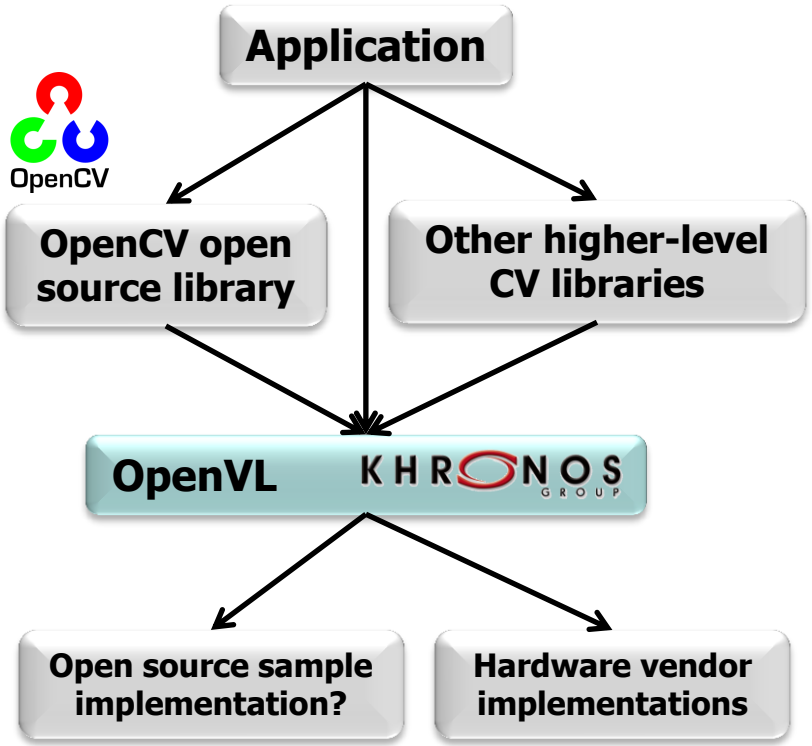
- **Widely used Computer Vision open source project**
 - Not an API definition, not managed by Khronos
- **Extensive functionality**
 - Used in academia, fast prototyping, some products
- **Traditionally runs on a single CPU**
 - Now many vendors are accelerating portions of OpenCV: OpenCL, CUDA, Neon
 - MulticoreWare open source CPU/GPU enabled OpenCV over OpenCL



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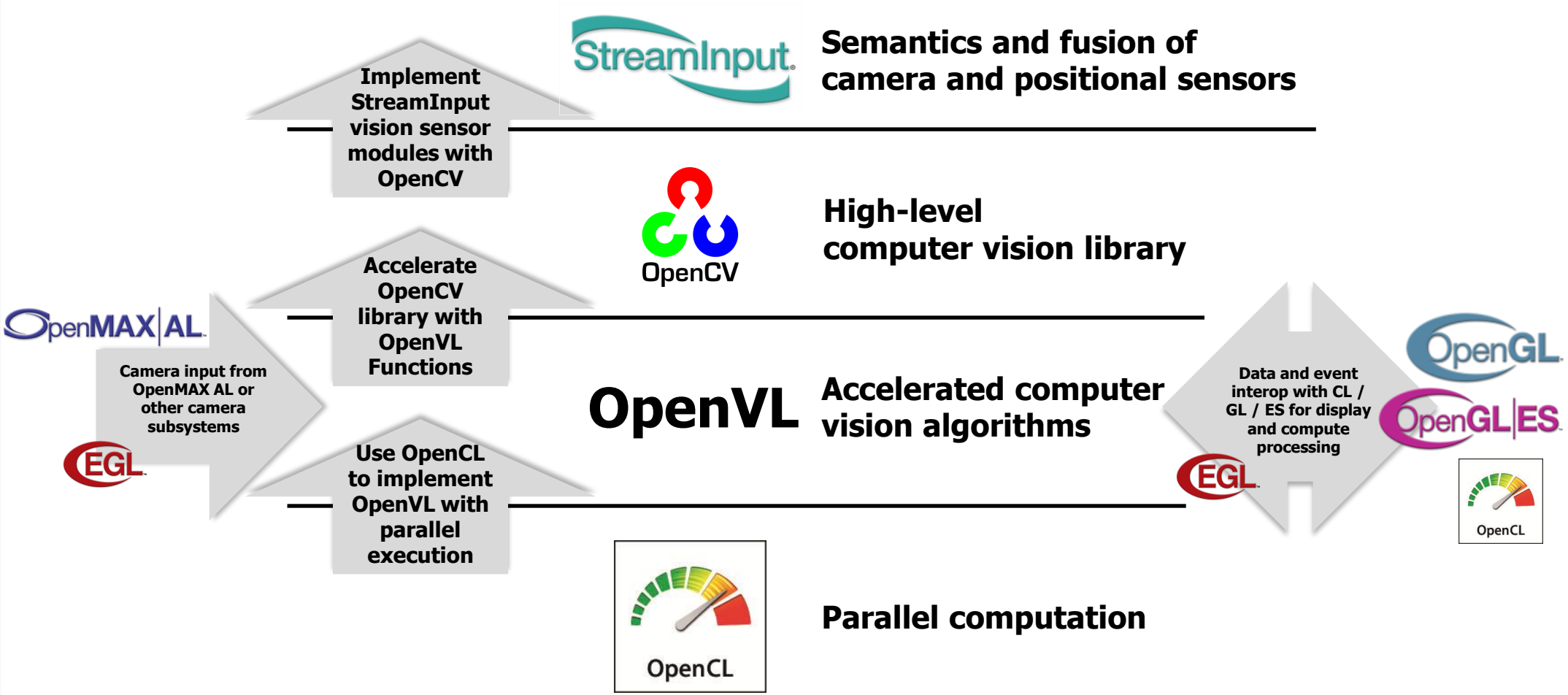
OpenVL

- **Vision Hardware Acceleration Layer**
 - Enable hardware vendors to implement accelerated imaging and vision algorithms
- **Diversity of efficient implementations**
 - From dedicated hardware pipelines to parallel programmable processors
- **Can be used by high-level libraries or applications directly**
 - Primary focus on enabling real-time vision apps on mobile and embedded systems
- **OpenCV will leverage OpenVL for acceleration**
 - OpenVL does not duplicate OpenCV functionality – JUST provides essential acceleration



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Possible Implementation of Vision Stack



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Requested Camera Extensions

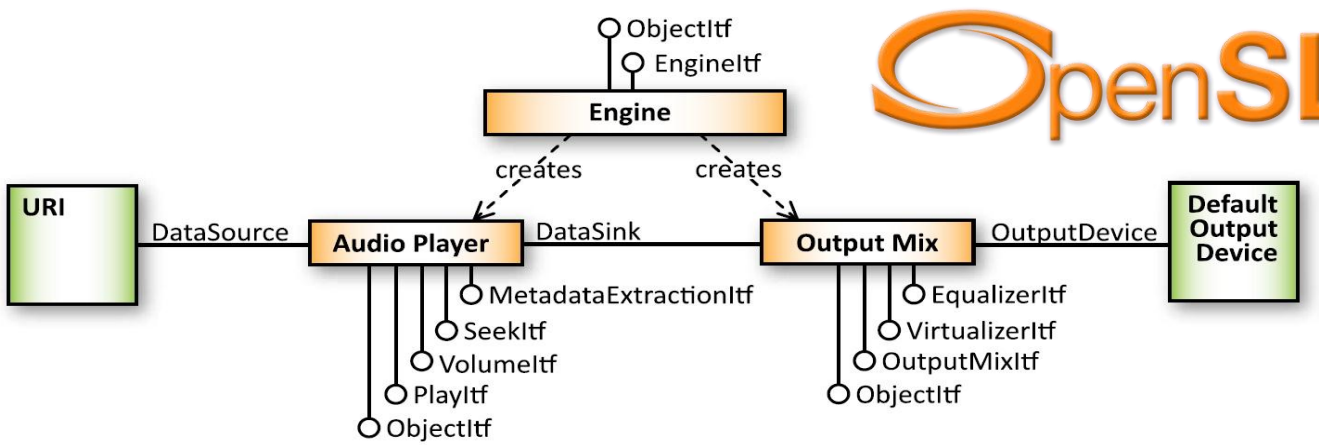
- **Query camera information**
 - Focal length (fx, fy), principal point (cx, cy), skew (s), image resolution (h, w)
 - Spatial information of how cameras and sensors are placed on device
 - Calibration and lens distortion
- **ROI extraction**
 - From wide angle and fish-eye lenses
- **FCAM++ - Extensive exposure parameters in single or burst mode**
 - Shutter, aperture, ISO, white balance, frame rate, focus modes, resolution
 - Synchronization with other system sensors
- **Data output format control**
 - Grayscale, RGB(A), YUV
 - Access to the raw data e.g. Bayer pattern

OpenMAX AL™

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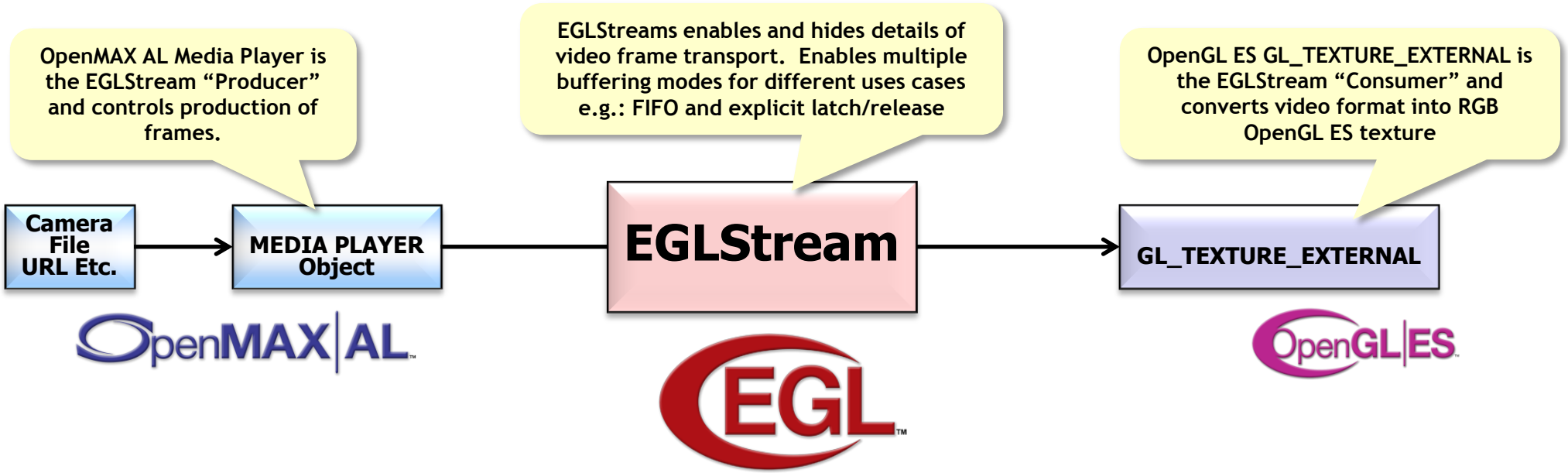
OpenSL ES – Advanced Audio

- **OpenSL ES does for audio what OpenGL ES does for graphics**
 - Advanced audio functionality from simple playback to full 3D positional audio
- **Object-based native audio API for simplicity and high performance**
 - Same object framework as OpenMAX AL
 - Reduces development time
- **Attractive alternative to open source frameworks**
 - Tightly defined specification with full conformance tests
 - Robust application portability across platforms and OS



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EGLStream – Video/Graphics Interop



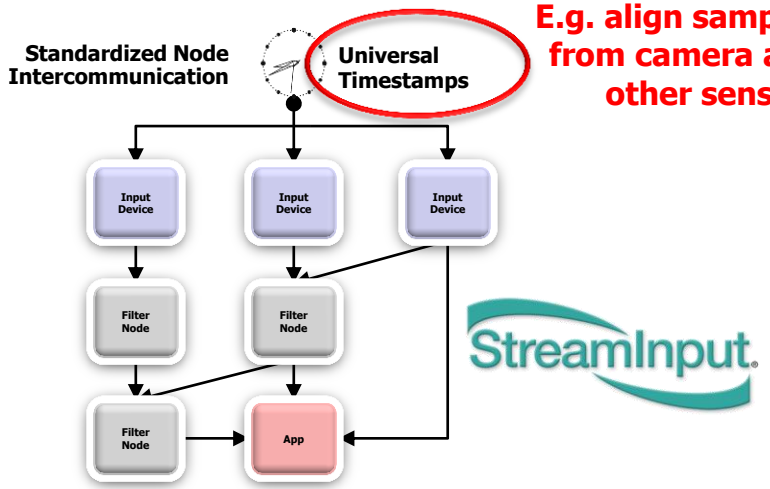
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Portable Access to Sensor Fusion

Apps request semantic sensor information
StreamInput defines possible requests, e.g.
"Provide Skeleton Position" "Am I in an elevator?"



Advanced Sensors Everywhere
RGB and depth cameras, multi-axis motion/position, touch and gestures, microphones, wireless controllers, haptics keyboards, mice, track pads



E.g. align samples from camera and other sensors

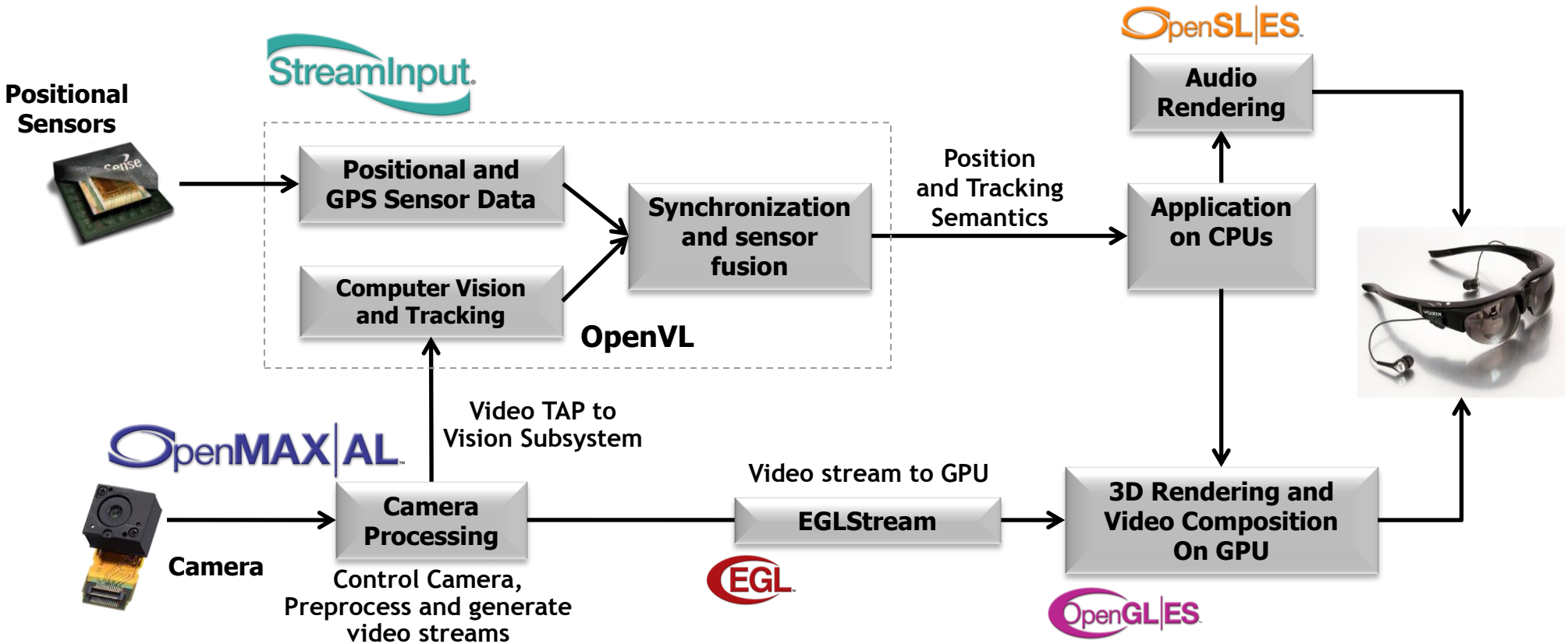


Apps Need Sophisticated Access to Sensor Data
Without coding to specific sensor hardware

Processing graph provides sensor data stream
Utilizes optimized, smart, sensor middleware
Apps can gain 'magical' situational awareness

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Example use of Khronos APIs in AR



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API Adoption



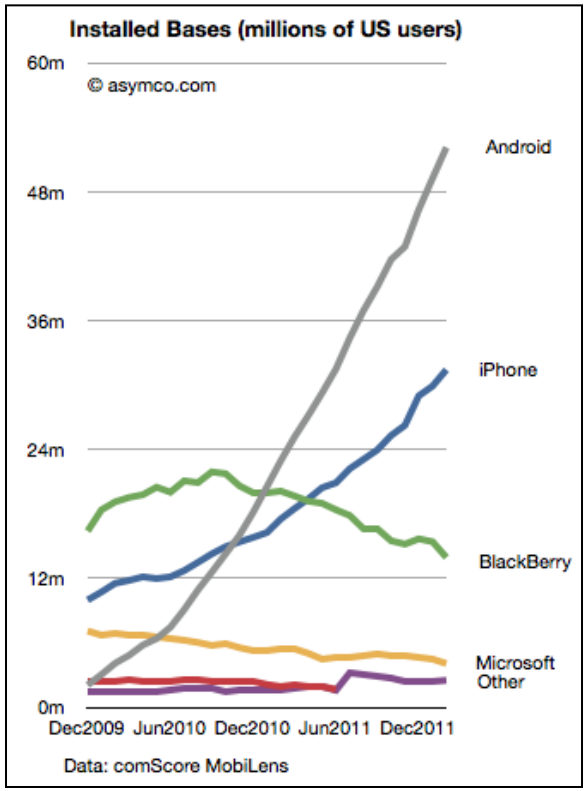
OpenGL ES	**OpenGL ES 2.0 Shipping - Android 2.2**
OpenSL ES	**OpenSL ES 1.0 Shipping – Android 2.3**
OpenMAX AL	**OpenMAX AL 1.0 Shipping - Android 4.0**
EGL	**EGL 1.4 Shipping under SDK -> NDK**
WebGL	**Chrome will have WebGL. Opera and Firefox WebGL now**



OpenGL	**OpenGL 3.2 on MacOS**
OpenCL	**OpenCL 1.1 on MacOS**
OpenGL ES	**OpenGL ES 2.0 on iOS**
WebGL	**Can enable on MacOS Safari iOS5 enables WebGL for iAds**



Mobile Operating Systems



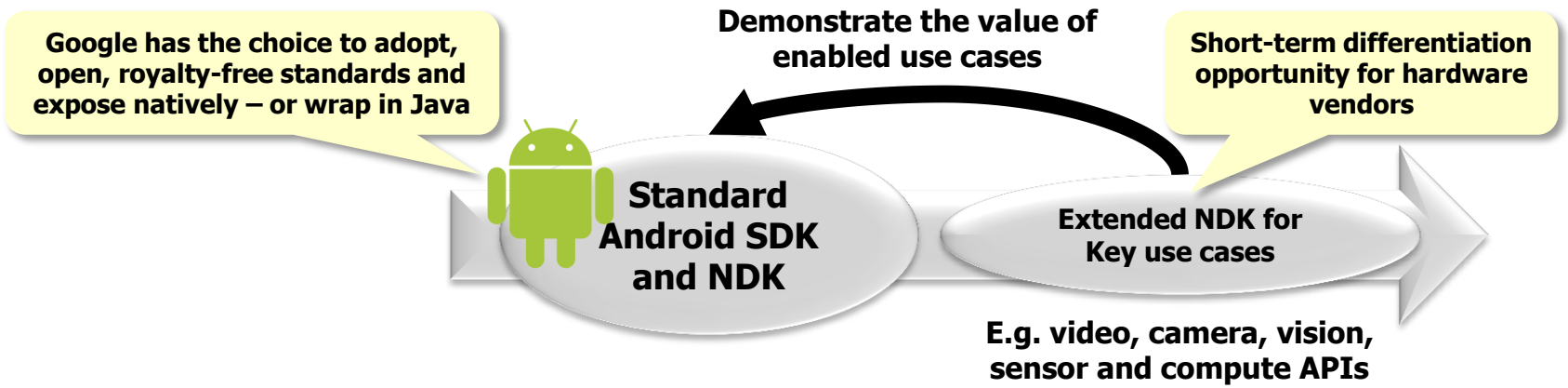
Microsoft Windows RT:

- **Only Microsoft native APIs**
- **HTML5 but not yet WebGL**

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Extended Native APIs on Android

- **Native APIs can be shipped as NDK extensions before Google Adoption**
 - Do not break/change existing Google APIs
- **Khronos open standard APIs have strong momentum in silicon**
 - Google has choice to adopt into standard platform to eliminate fragmentation
 - Exposed directly – or wrapped in Java binding
- **Extended APIs can be used by:**
 - Bundled apps, Market apps with API selection
 - Multiple APKs behind single multi-APK SKU



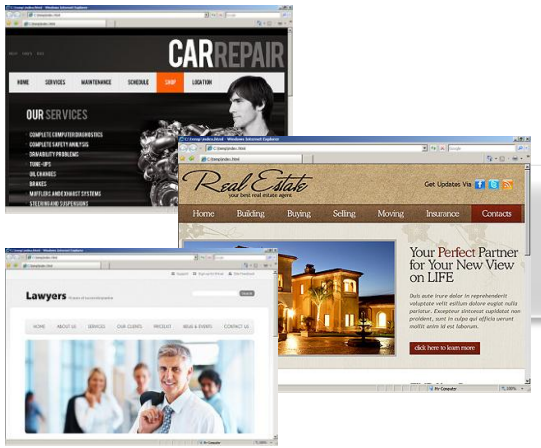
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HTML5 – Cross OS App Platform

- **Increasing diversity of devices creates a demand for a true cross OS programming platform**
- **BUT need more than "more HTML"**



Traditional Web-content



HTML

Rich Experiential Processing

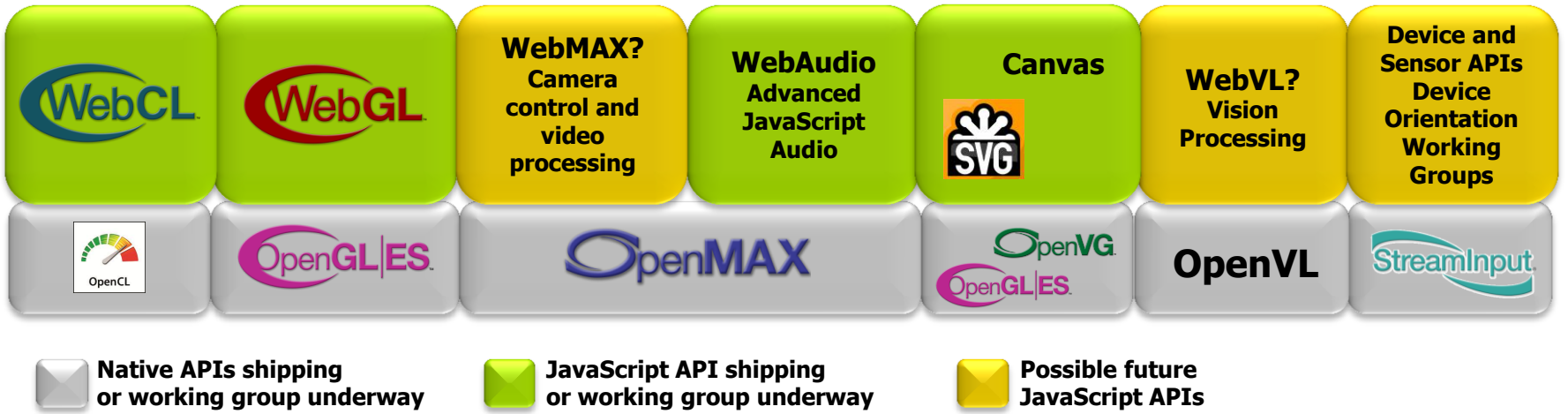
Multi-core CPUs
Rich 2D and 3D GPU
GPU Computing
Multiple HD cameras
Image and vision processing
Video encode/decode
Audio encode/decode
Inertial and positional sensors

How can the Browser rapidly assimilate such diverse functionality?

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Leveraging Proven Native APIs into HTML5

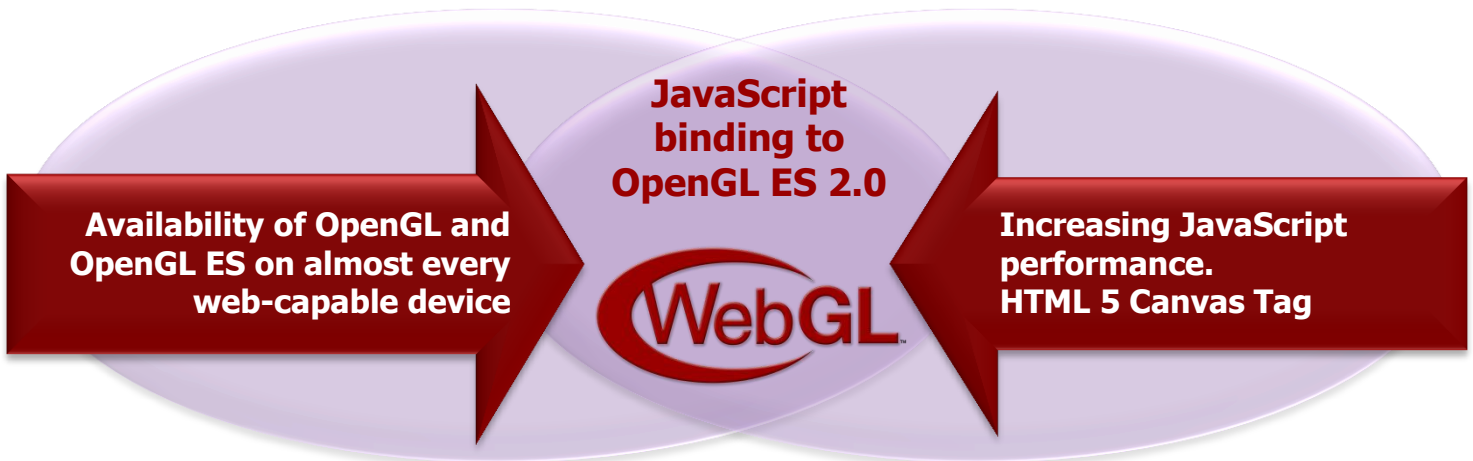
- **Leverage native API investments into the Web**
 - Faster API development and deployment
 - Familiar foundation reduces developer learning curve
- **Khronos and W3C creating close liaison**
 - Multiple potential joint projects



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WebGL – 3D on the Web – No Plug-in!

- **Historic opportunity to bring accelerated 3D graphics to web**
 - WebGL defines JavaScript binding to OpenGL ES 2.0
- **Leveraging HTML 5 and uses <canvas> element**
 - Enables a 3D context for the canvas
- **Low-level foundational API for accessing the GPU in HTML5**
 - Flexibility and direct GPU access - support higher-level frameworks and middleware
- **WebGL 1.0 Released at GDC March 2011**
 - Mozilla, Apple, Google and Opera working closely with GPU vendors



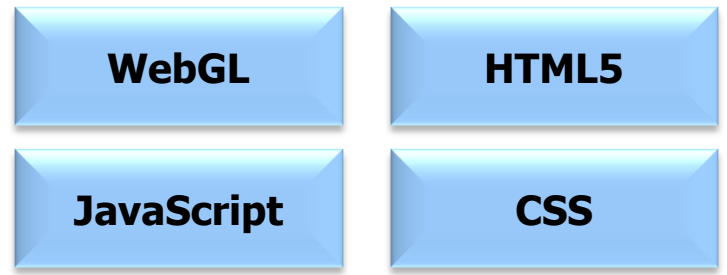
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WebGL Implementation Anatomy

Content downloaded from the Web. Middleware can make WebGL accessible to non-expert 3D programmers



Browser provides WebGL functionality alongside other HTML5 specs - no plug-in required

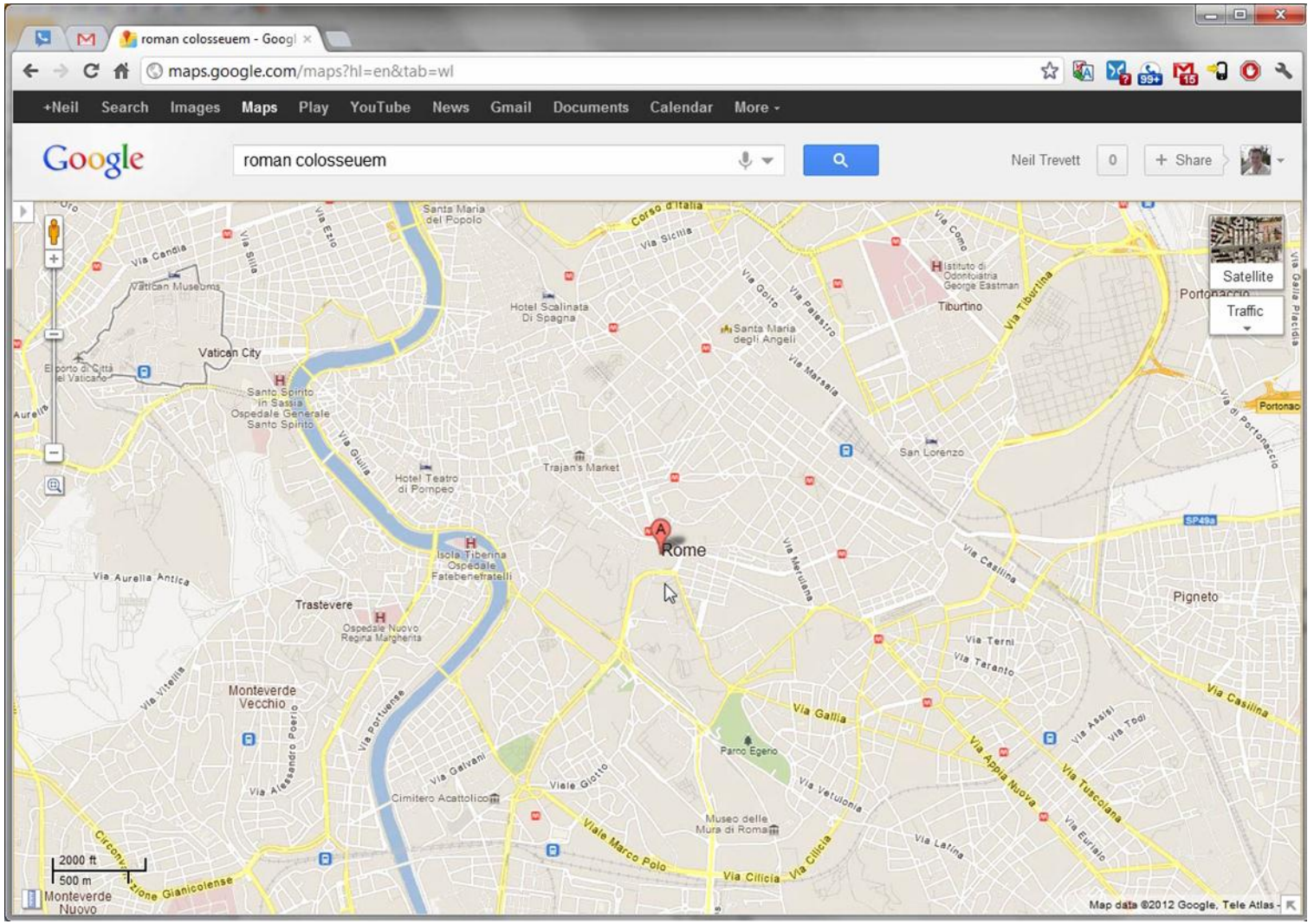


OS Provided Drivers. WebGL on Windows can use Google Angle to create conformant OpenGL ES 2.0 over DX9



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WebGL – Being Used by Millions Every Day



WebGL and Security

- **WebGL is Architecturally Secure**
 - NO known WebGL security issues
 - Impossible to access out-of-bounds or uninitialized memory
 - Use of cross-origin images are blocked without permission through CORS
 - Browsers maintaining black lists - used if unavoidable GPU driver bugs discovered
- **DoS attacks and GPU hardening**
 - Draw commands can run for a long time -> unresponsive system
 - Even without loops in shaders
 - WebGL working closely with GPU vendors to categorically fix this
 - Short term: mandate ARB_robustness and associated GPU watchdog timer
 - **Longer term: GPUs need robust context switch and pre-emption**

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WebCL – Parallel Computing for the Web

- **JavaScript bindings to OpenCL APIs**
 - JavaScript initiates OpenCL C Kernels on heterogeneous multicore CPU/GPU
- **Stays close to the OpenCL standard**
 - Maximum flexibility to provide a foundation for higher-level middleware
- **Minimal language modifications for 100% security and app portability**
 - E.g. Mapping of CL memory objects into host memory space is not supported
- **Compelling use cases**
 - Physics engines for WebGL games, image and video editing in browser
- **API definition underway – public draft just released**
 - https://cvs.khronos.org/svn/repos/registry/trunk/public/webcl/spec/latest/index.html



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WebCL Demo

http://www.youtube.com/user/SamsungSISA#p/a/u/1/9Ttux1A-Nuc



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Web Apps versus Native Apps

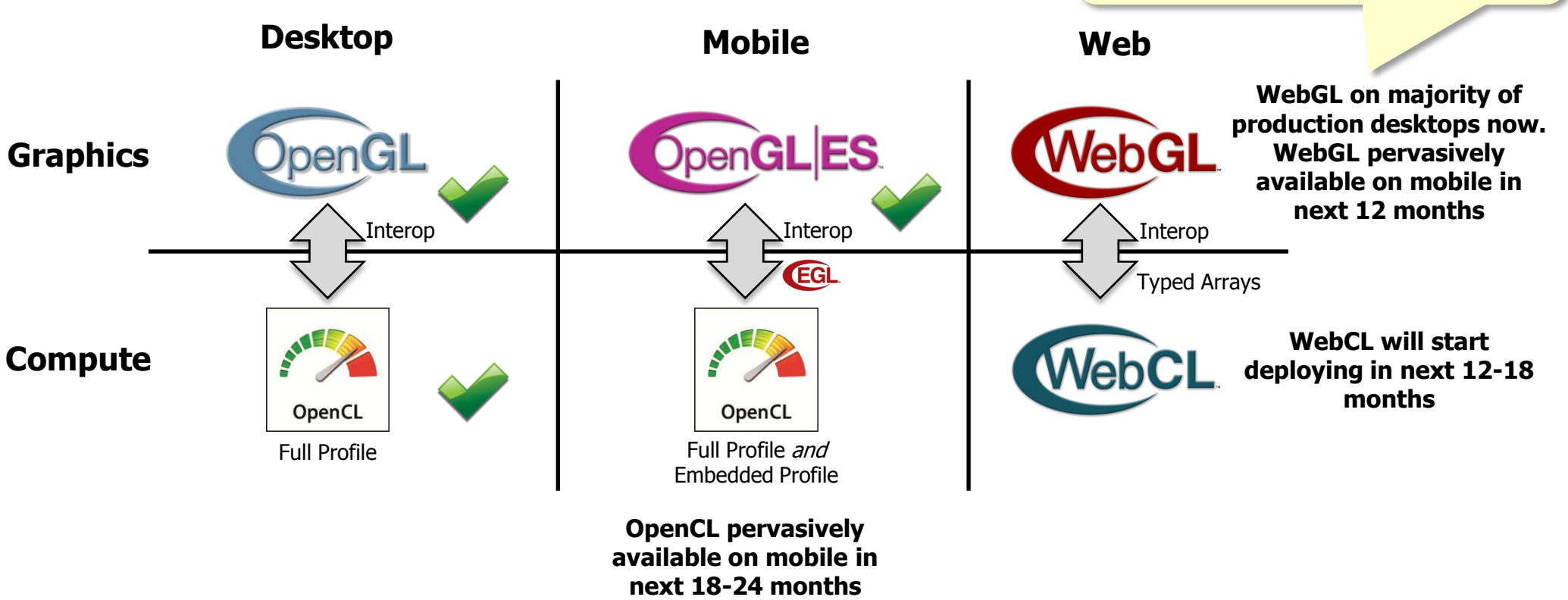
- **Mobile Apps have functional and aesthetic appeal**
 - Beautiful, responsive, focused
- **HTML5 with GPU acceleration can provide the same level of "App Appeal"**
 - Highly interactive, rich visual design
- **Using HTML5 to create 'Web Apps' has many advantages**
 - Web app is searchable and discoverable through the web
 - Portable to any browser enabled system
 - Same code can run as app or as web page
 - Not a closed app store – no app store 'tax'
- **How soon will we be able to write apps such as AR in HTML5?**



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Expanding Platform Reach for Graphics and Computation

Production Browsers Shipping with WebGL:
Desktop - Chrome, Firefox, Opera, Safari
Mobile - Opera and Firefox
Apple iOS Safari uses WebGL for iAds



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Cross-OS Portability





Microsoft
Windows RT

HTML	HTML/CSS WebGL	HTML/CSS WebGL	HTML/CSS No WebGL
SDK	Dalvik (Java)	Objective C	C#
C/C++	OpenGL ES	OpenGL ES	DirectX

HTML5 provides cross platform portability. GPU accessibility through WebGL available soon on ~90% mobile systems

Preferred development environments not designed for portability

Native code is portable- but apps must cope with different available APIs and libraries

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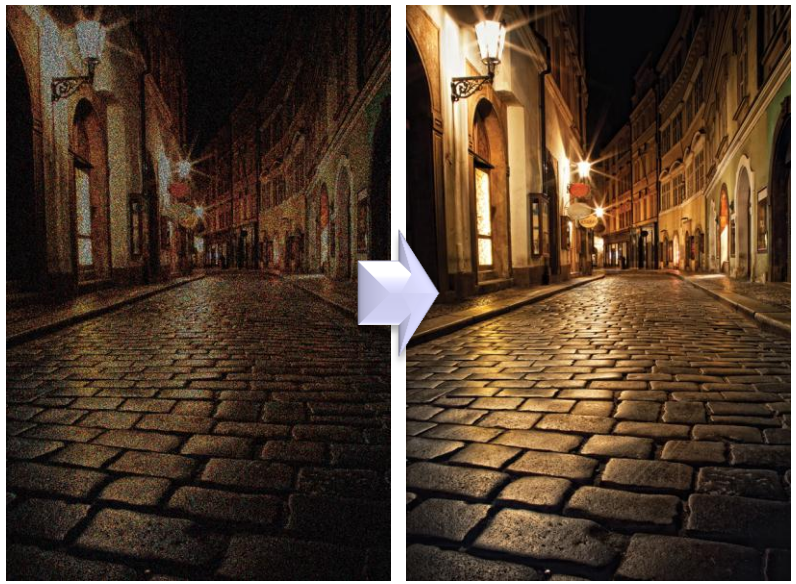
Summary

- Advances in SOC silicon processing are enabling significant new use cases
- Architectural shifts, such as unified memory, are creating challenges and opportunities for applications and the APIs that enable them
- Holistic cooperation between hardware and software needed to deliver increasing computational loads in a fixed power budget
- Dynamic tension between platform vendors that want captive apps and developers that benefit from cross platform portability
- Mobile operating systems lag in exposing the latest SOC capabilities which creates functional differentiation opportunities
- Cooperative API standards eliminate roadblocks to mobile industry growth

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Thank You!

See you back at 11:10AM



HOT CHIPS

ArcSoft®

ArcSoft Multi-Frame Technologies

Hot Chips 2012

Sean Mao, VP Marketing
Advanced Imaging Technologies

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ArcSoft Overview

- Founded in 1994
- HQ in Fremont, CA
- 900+ employees worldwide
- Photo & Video software
- Markets served:

 Mobile, tablet, PC, DSC



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Industry Leaders Choose ArcSoft







































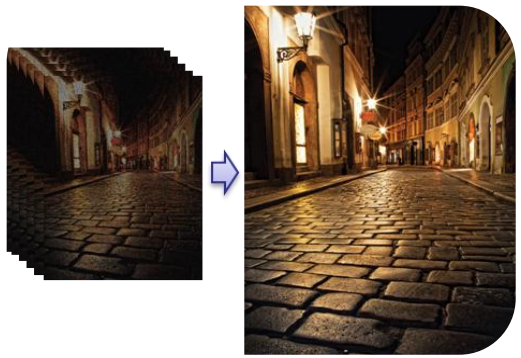


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ArcSoft Imaging Technologies

- **Adopted by major camera phone vendors and digital camera vendors**
- **Leverages various forms of hardware capabilities**
 - CPU, GPU, DSP, ISP, H/W Codec, Fast RAM, DMA, and other specialized hardware
 - Highly efficient ISP
- **Boosts value to the end product**
 - Better capture quality and speed performance
 - Better user experience
 - Differentiation



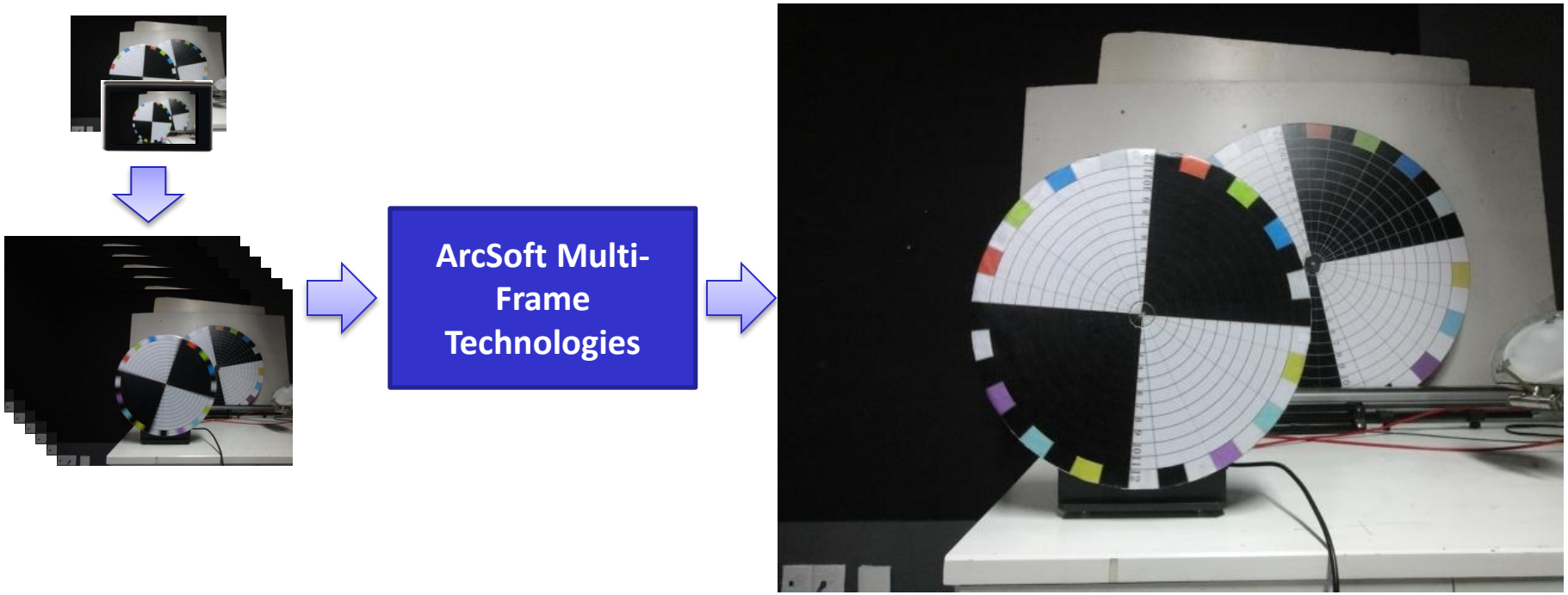




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ArcSoft Multi-Frame Technology Overview

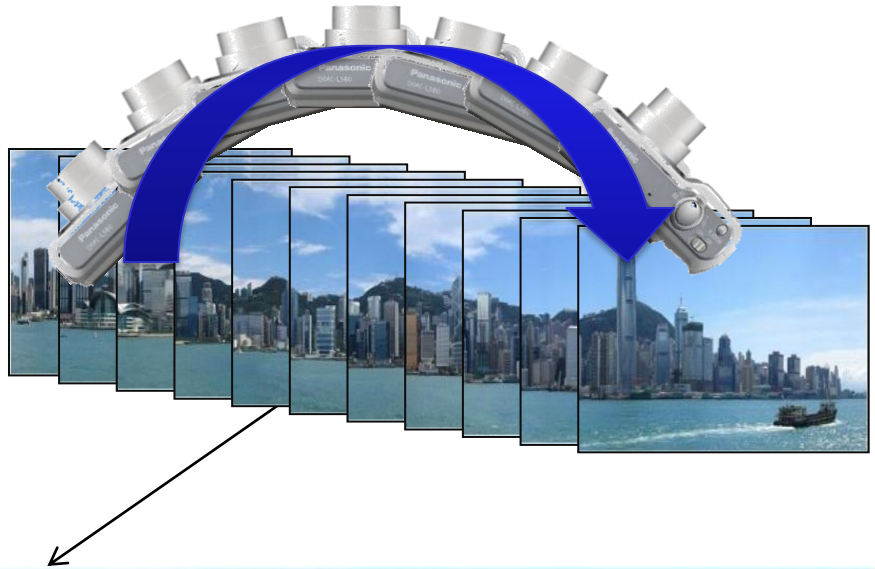
- Takes advantage of high speed burst capability in latest capture SOC
- Combines multiple image frames to achieve improved image quality and better experience



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ArcSoft Multi-Frame Technology Portfolio

- Multi-Frame Night Shot
- Panorama BurstCapture
- Multi-Frame Anti-Shaking
- High Speed HDR
- PiClear (auto object removal)
- PicBest (optimal portrait composition)
- More…





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Achieve Better Quality With Multi-Frame

- Brighter
- Clearer
- Better resolution



COMPARING WITH SONY DSC TX-10

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Hardware Requirements

- **Fast burst capture capability (>15 FPS)**
- **Continuous burst to more than 300 shots and stop at any time**
- **For each capture in the burst**
 - H/W noise filter enabled
 - Output in YUV formats
 - Capability to do bracketing

 e.g. void setEvBracketCapture(float[]); // In NvCamera
 - Capability to change the capture parameters (3A, ISO, Gain, etc)

 e.g. void void setExposureTime(int); // In NvCamera
 - Capability to lock the capture parameters

 e.g.

 void setAutoExposureLock(boolean lock); // In NvCamera

 void setAutoWhiteBalanceLock(boolean lock); // In NvCamera

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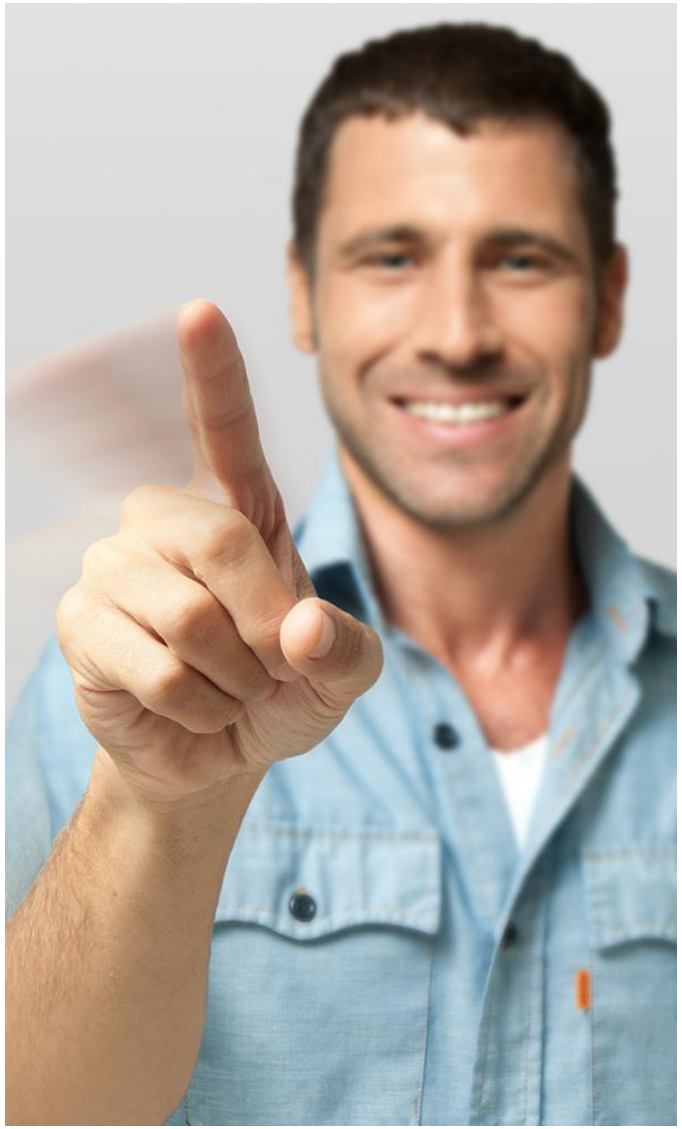
Challenges and Expectations

- **Quality of the each frame in the burst is not well-tuned sometime, especially when captured with non-3A parameters**
- **Image frames sometime are not consistent even with all capture parameters locked**
- **Need downsized image frames passed from ISP**
- **Need Bayer RAW output**
- **Need hardware-based math functions especially for matrix operations**
 - e.g. add, subtract, multiply, absolute difference, division, max, min, linear gradual blend, etc..

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Thank You For Your Time



HOT CHIPS

eyeSight™

Touch-free technology

Itay Katz
Founder and CTO

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Overview

eyeSight's groundbreaking Touch Free technology provides an enhanced user experience, allowing to easily and intuitively control a variety of devices using simple hand gestures.

eyeSight's Natural User Interface solution utilizes the device's standard 2D camera, along with advanced real-time image processing and machine vision algorithms, to track the user's hand gestures and convert them into actions.

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Components of eyeSight's Gesture recognition technology:

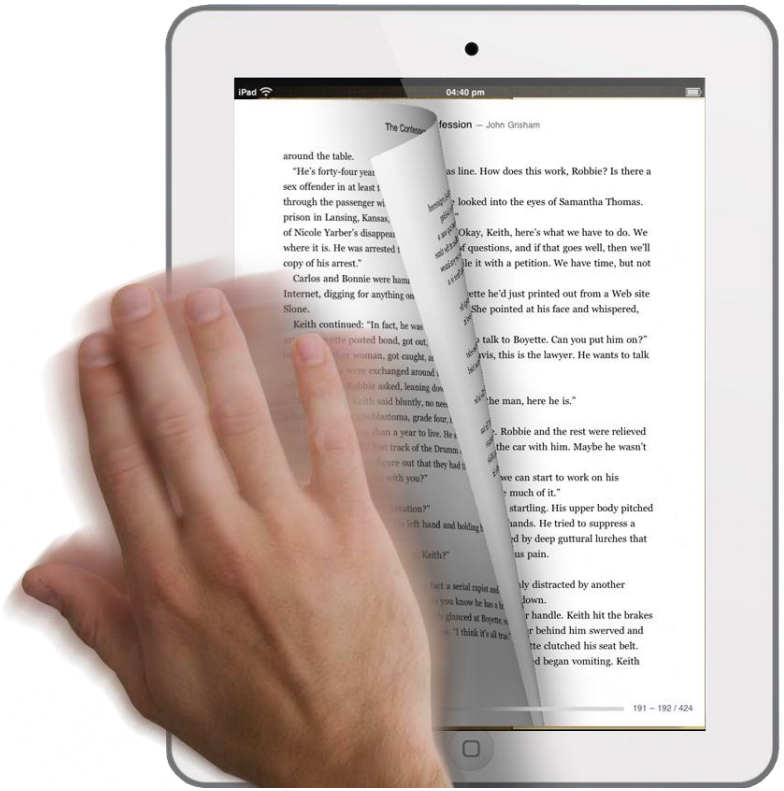
- Directional gestures detection
- Real-time hand / fingertip tracking
- Face detection and tracking (multiple users)
- Hand signs; "OK", "Like" etc.



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Implementation Challenges of such technologies:

- Very high processing requirements
- Memory Throughput
- Real-time performance



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Solutions: Managing performance

- **Algorithm- the key tool for minimizing performance**
- **Target specific optimizations**
 - Instrinsics – using special instructions
 - ISA Extensions: x86 SSE, ARM NEON
 - Assembly
- **GPGPU – OpenCL**



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Solutions: Coping with memory throughput

- **Image processing algorithms require reading/writing the video many times, placing a lot of load on the memory subsystem. Reading a 720p YUV422 streams just once requires 55 Mbytes/Sec.**
- **DMA – not usable in most systems, since there are no tightly-coupled memories.**
- **It is key to minimize the number of passes on the video data.**
- **Designing for Cache**
 - Minimize data footprint
 - Locality
 - Automatic pre-fetching
 - Software pre-fetching

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Solution: Handling real-time performance

- Most systems are non-deterministic:
 Caches, other processes, O/S behavior
- Algorithms require more processing when there's "action" in the video
- This makes the instantaneous performance requirements vary greatly
- As a result, it is not possible to guarantee hard real-time performance
- Instead, our solution is design to be soft real-time, and to handle real-time violations
- One challenge is the lack of standardized high-precision timers to allow software to monitor execution time

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Platform portability - Challenges:

Challenges:

- **Maintaining a single code base across multiple products, OS types and compilers**
- **Stay up to date with recent OS version releases**
- **Maintain backward compatibility**
- **Maintaining pixel portability**

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Platform portability - Solution:

Solution:

- Working with automated tools for each core code change
- Maintain strict coding conventions to avoid using platform specific libraries
- Use cross platforms frameworks such as OpenCL
- Work with a configurable device abstraction layer to keep platform specific code from migrating into different platforms or devices
- Using a framework developed in eyeSight we can convert any video stream, any resolution or format (including IR), to a single representation that serves our algorithms

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Thank you.
www.eyeSight-tech.com
eyeSight™



HOT CHIPS

metaio
AUGMENTED SOLUTIONS

Augmented Reality

Hot Chips 2012

Ben Blachnitzky
Director R&D, Metaio

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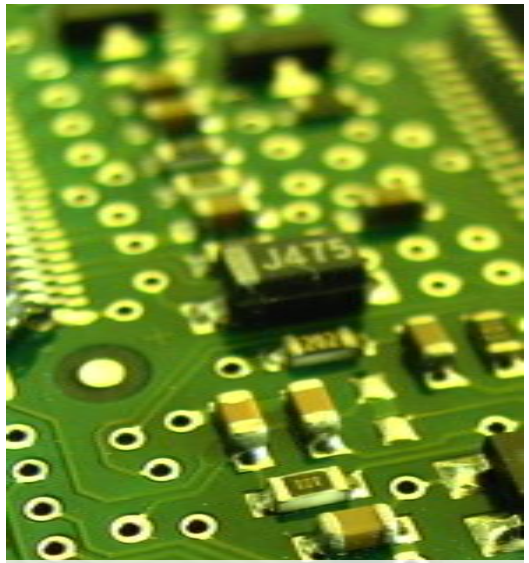
- Founded 2003 out of computer vision research
- Privately held, independently financed
- 500+ B2B customers worldwide
- 85+ people working in Munich (HQ) and San Francisco
- 10,000+ active developers worldwide
- Extensive R&D department with 100+ patents across 38 different families
- 200+ mobile apps running on metaio technology





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From Hardware to Software to End User

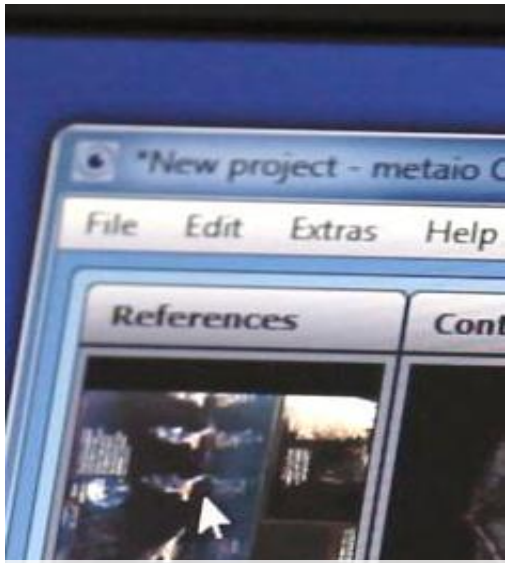


Hardware
AR Devices

ST ERICSSON

ARM

Texas Instruments

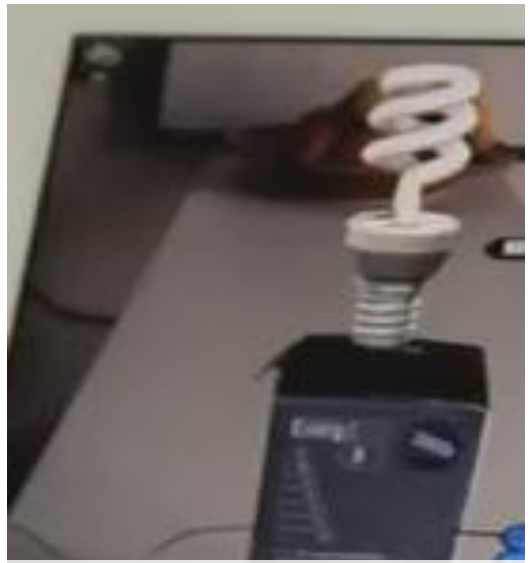


Software
AR Applications

metaio Mobile SDK

metaio Web SDK

metaio PC SDK



Content
AR Usage

UCHIDA · CYBERNET · ON-X

the mass media lab · UNIJA

DNP Dai Nippon Printing · SENAI-RJ · eria

j.spot



Users
AR Monetization

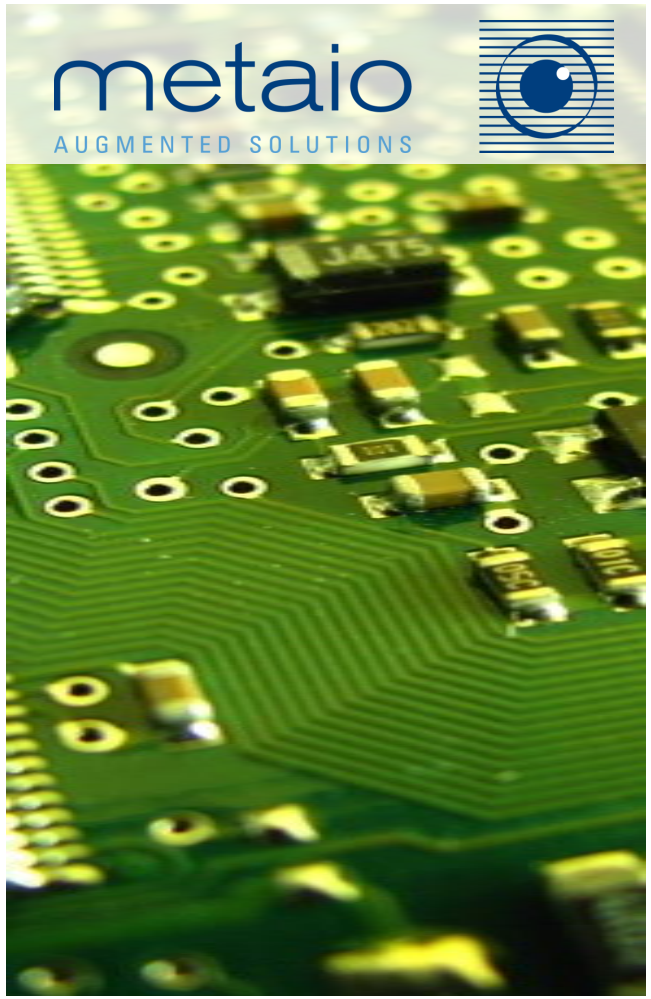
junaio powered by metaio

junaio certified developer

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General Milestones

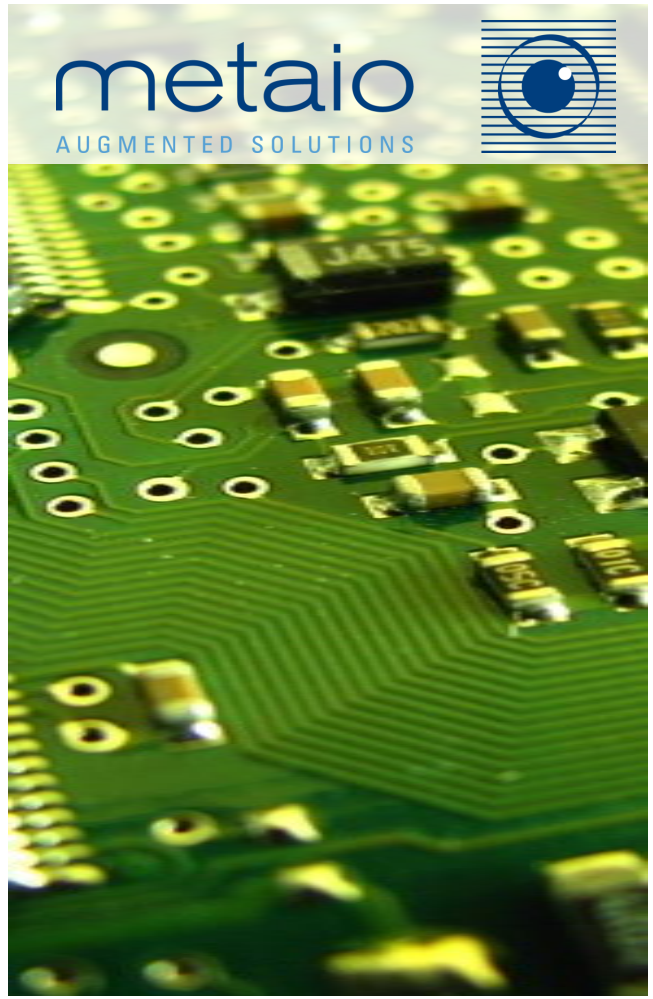
- **Oct. 2011: Won ISMAR tracking competition with pure mobile marker-less tracking**
- **Dec. 2011: mobile SDK 3.0 release**
 - Advanced visual tracking of 2D and 3D objects
 - Gravity aware AR
 - Optimized AR-pipeline for major mobile chipsets (ARM, ST-Ericsson, Texas Instruments)
- **February/March 2012: Augmented City Platform at MWC and SDK 3.1**
 - Advanced 3D object tracking
 - Visual search technology
 - Further hardware optimization on AR-pipeline
- **Estimated Q4 2012: mobile SDK 4.0**



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Achievements and Challenges

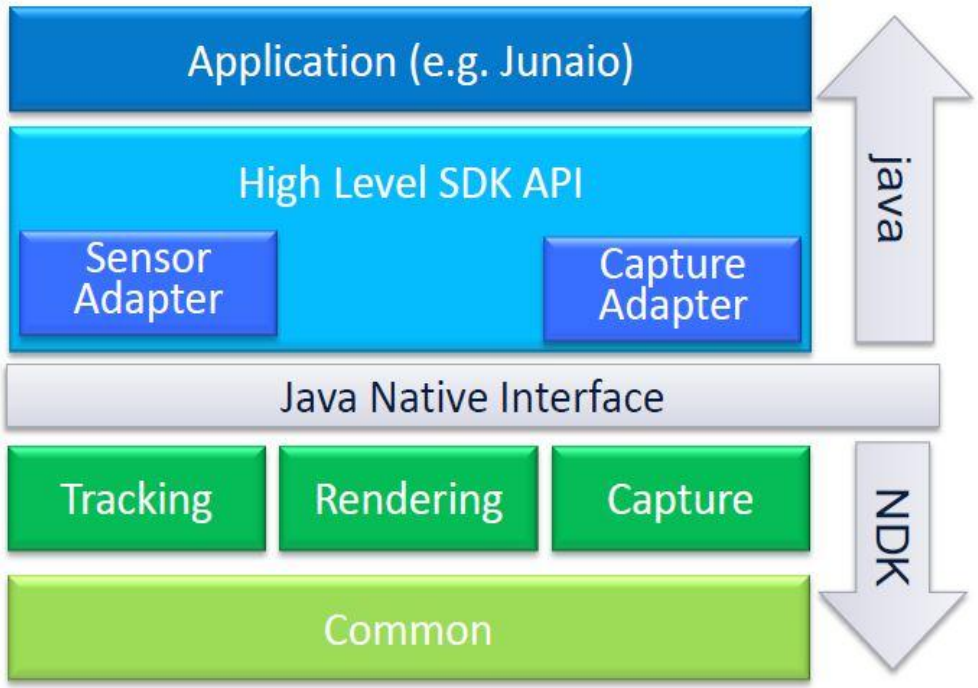
- **From marker-tracking to full 3D Object Tracking on mobile in only 14 months**
- **Low level optimizations:**
 - Leveraging SIMD extensions (e.g. NEON) for certain computer vision tasks
 - Memory constraints and optimizations especially for large client based visual search
 - General pipeline optimizations and leveraging modern multi-core architectures
 - Optimized camera access for e.g. high-resolution visualization images and lower resolution tracking images
- **Challenges:** Battery consumption & extending the limits of tracking in AR so that it becomes natural for consumers

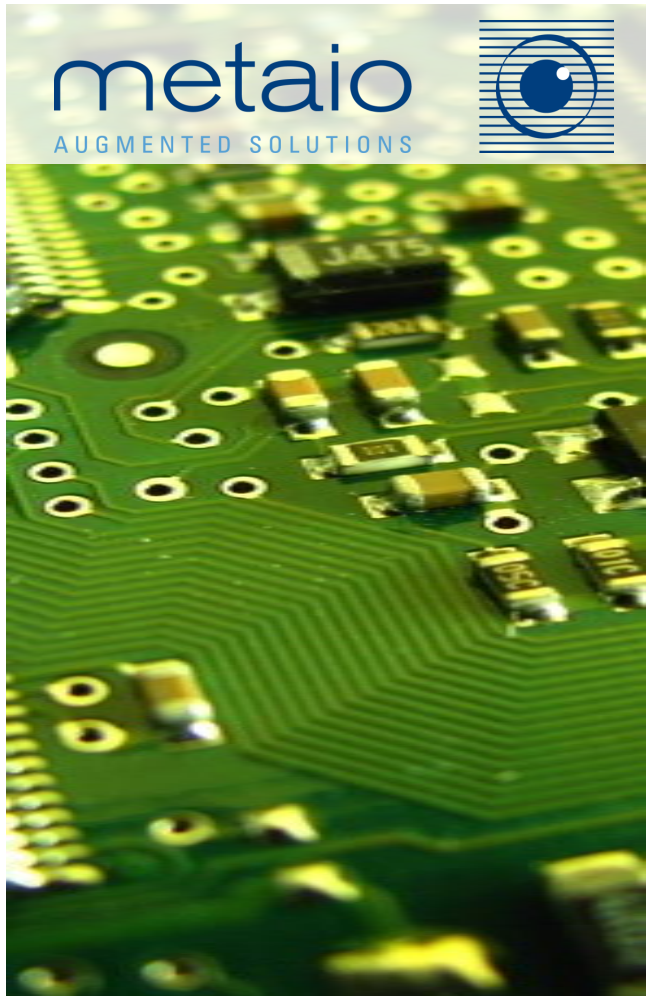


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High-level Overview of Mobile SDK

- **Android Developer Perspective**
 - Java IF for straightforward application development
 - Computational-intensive operations in NDK
 - JNI provides language interoperability





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Multiple Object AR

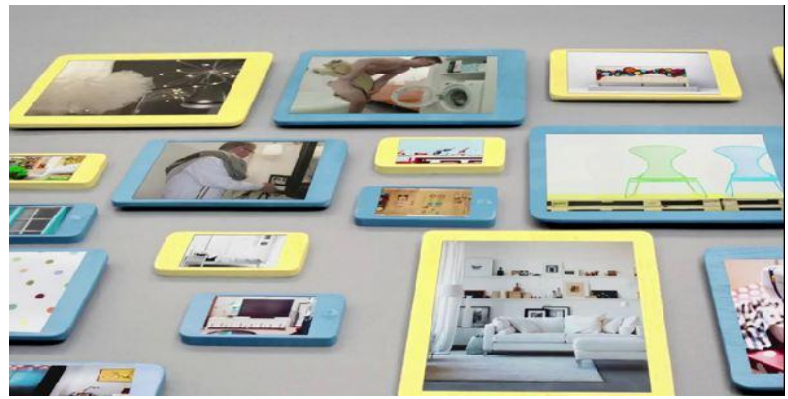
- More than 40 instances of client-based real-time image detection made possible through specific optimized algorithms
- Activation and recognition speed comparable to Quick Response (QR)



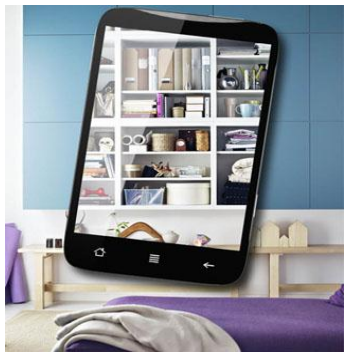
http://www.youtube.com/watch?v=QQ8HNXtl7jQ&feature=player_embedded

http://creativity-online.com/news/mccannerickson-gives-new-ikea-catalog-a-vitamin-pill/236165





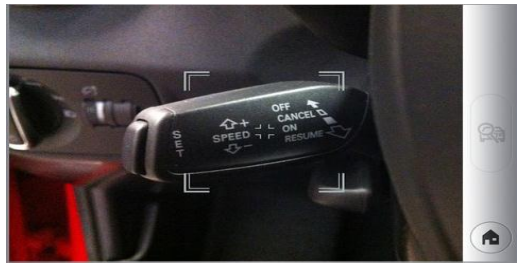




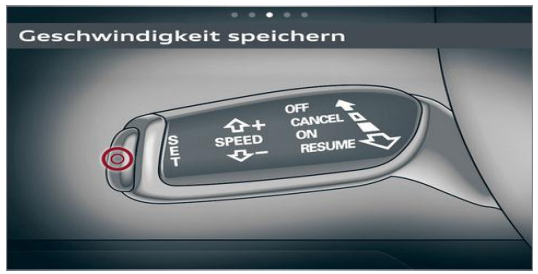
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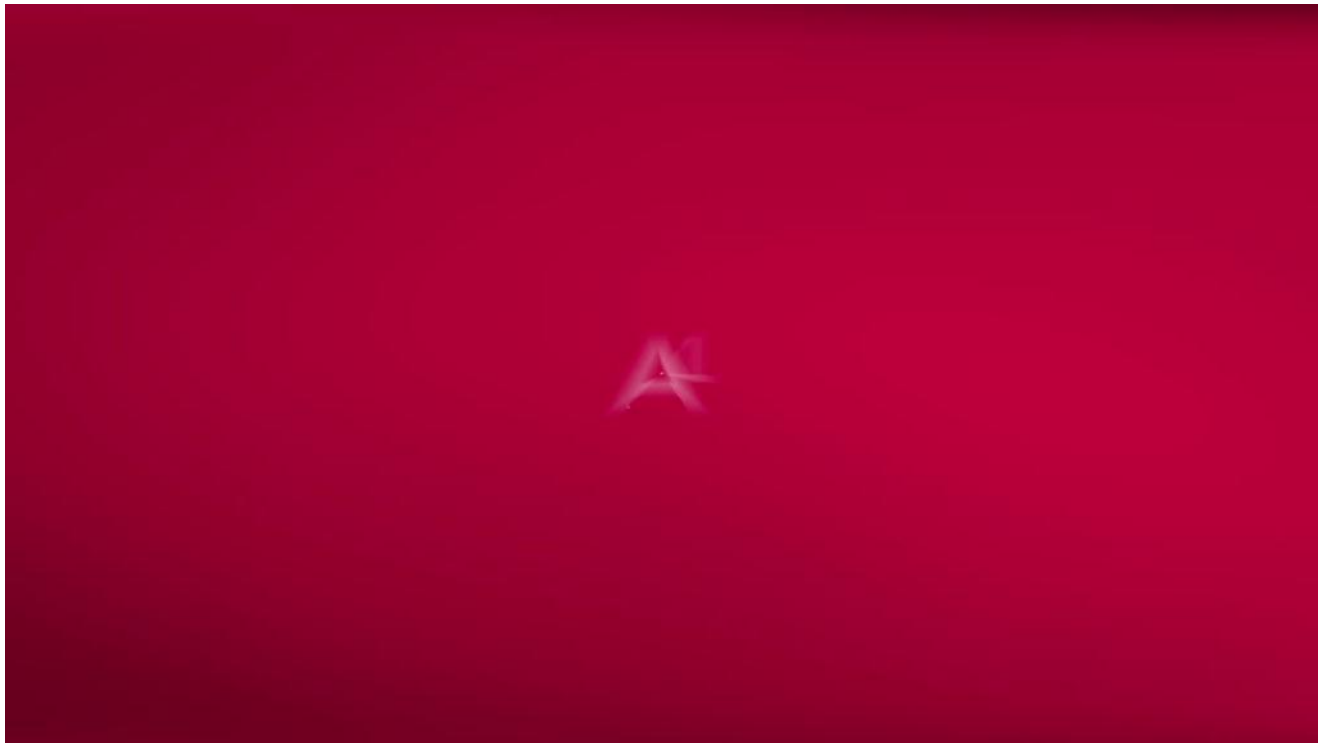
Useful AR Optimizations











http://www.youtube.com/watch?v=DMg4UUCaQdw

- **100+ images detected and recognized**
- **Same algorithms and technology are freely available to mobile developer ecosystem**

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AR Enhanced Print Media (Mobile AR)



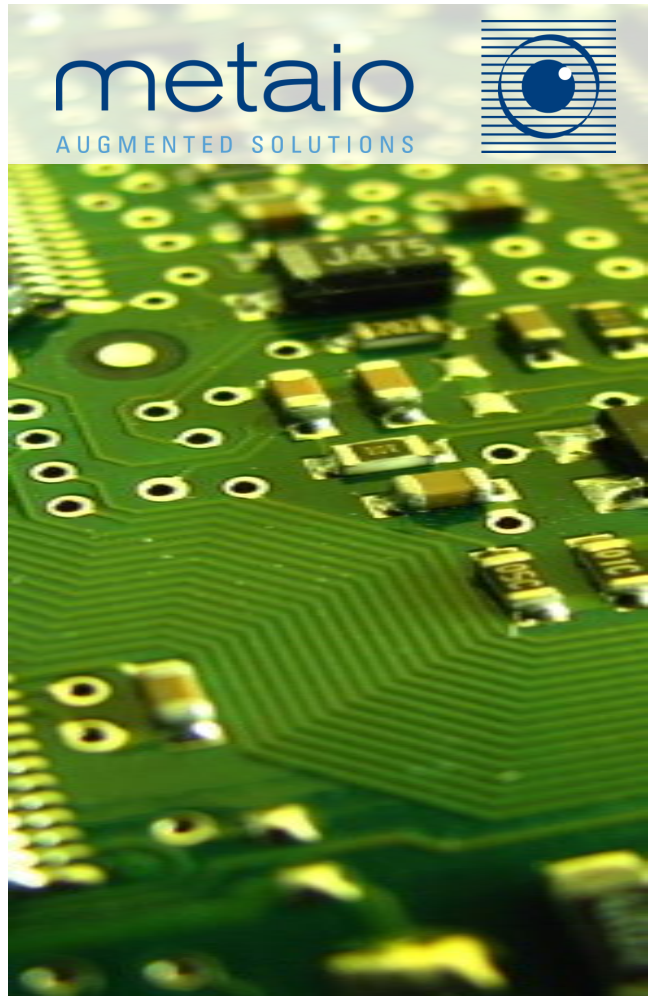
http://www.youtube.com/weltderwunderadsales#p/f/3/KZS1Q3I0a9Q

- Powering "AR-Lite" cloud-based experiences that should be accessible in nearly all connectivity environments
- Current adopters: The Atlantic, Axel Springer, Burda, Süddeutscher Verlag, USA Today
- **<u>+10 million</u> copies of AR enhanced magazines are powered by junaio cloud infrastructure**

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API | Hardware Wish List

- **One Computer Vision hardware abstraction layer for Android and iOS**
- **Native/Advanced camera access across different platforms:**
 - Visualization image and tracking image
 - Hardware optimized image pre-computations/conversions
 - Full control of camera parameters such as shutter, brightness, (auto-) focus
 - Very fast texture upload to renderer for camera image
 - Platform independent parallelization approaches (SIMD and multi-core)
 - HW implementation for most important AR functions to address the battery consumption issue



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metaio

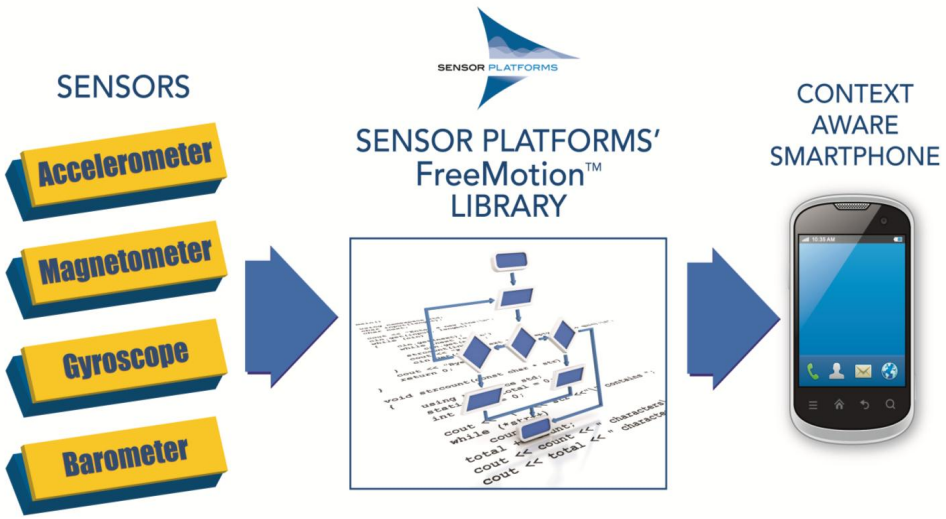
AUGMENTED SOLUTIONS

www.metaio.com



@twitt_AR **facebook.com/metaio** **augmentedblog.wordpress.com**

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HOT CHIPS

SENSOR PLATFORMS

Sensor Fusion

Mobile Platform Challenges and Future Directions

Jim Steele

VP of Engineering, Sensor Platforms, Inc.

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How Many Sensors are in a Smartphone?



- **Light**
- **Proximity**
- **2 cameras**
- **3 microphones (ultrasound)**
- **Touch**
- **Position**
 - GPS
 - WiFi (fingerprint)
 - Cellular (tri-lateration)
 - NFC, Bluetooth (beacons)
- **Accelerometer**
- **Magnetometer**
- **Gyroscope**
- **Pressure**
- **Temperature**
- **Humidity**

19

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Mobile Sensor Challenges



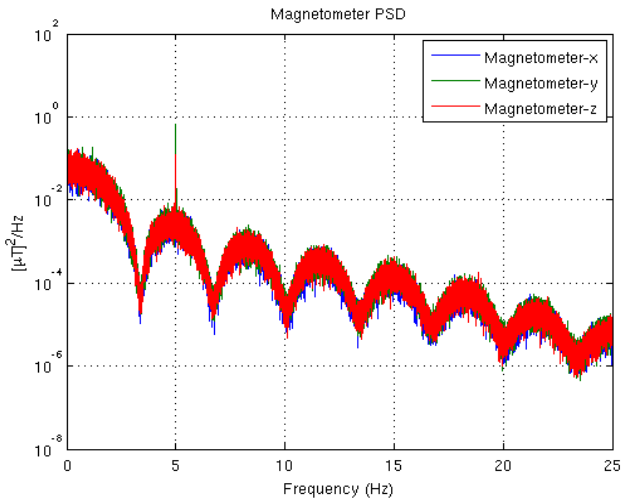
~90° compass error in the first Ice Cream Sandwich smartphone

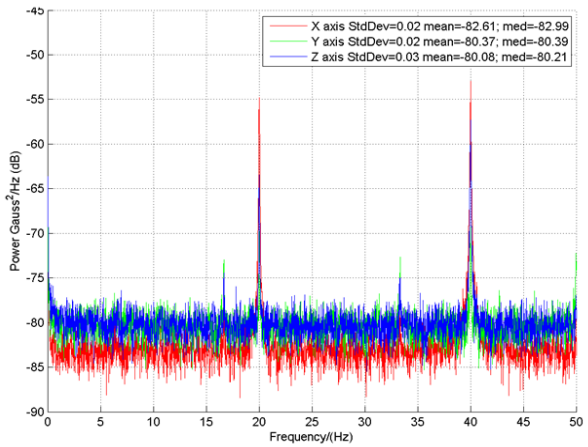
- **Underlying problems:**
- **Some sensor components lack repeatability**
- **RF and other PCB noise interaction with mag sensor**
- **Non-standard availability (no gyro, pressure, 2nd camera, …)**
- **Non-standard capability (resolution, update rate, …)**
- **Not fully specified (non-uniform gain, skew)**

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User Experience Across Platforms

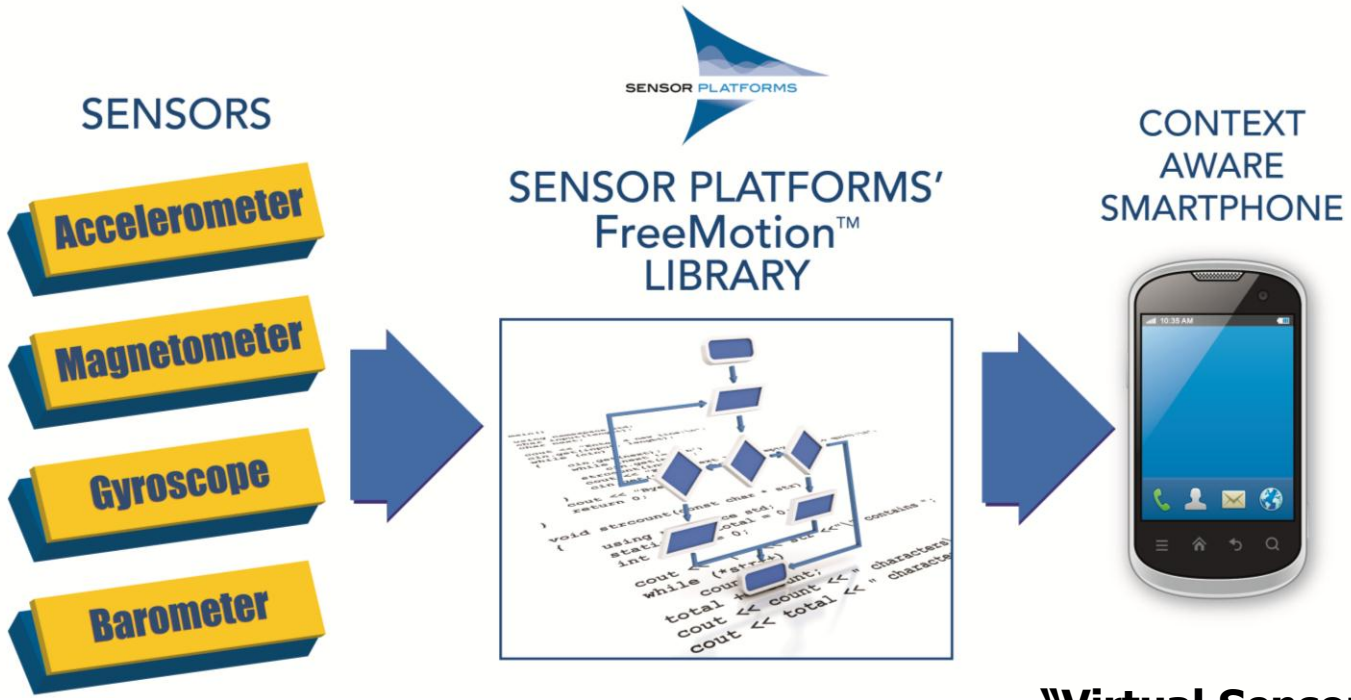
- **Heavy engineering burden to maintain consistency across system variations**
 - Hard and soft iron contents
 - Component selection for optimal price/performance
 - Different application processors (sensor hubs)
 - Different mobile OS
- **Validation efforts diffused over multiple platforms**





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Sensor Fusion Algorithms Solve Challenges



What can be measured
-acceleration
-magnetic field
-angular rate
-pressure

"Virtual Sensors"

What developers want
-quaternion
-gravity
-linear acceleration
-tilt

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Examples of Sensor Fusion

- **10-axis sensor fusion and background calibration**
 - Industry standard foundation for sensors
 - No user-intervention to keep sensors calibrated
 - Adjusts to changes in environment
- **Sensor data can be interpreted using algorithms**
 - Magnetometer → Compass (avoid magnetic anomalies)
 - Pressure → Altitude (avoid pressure anomalies)
 - Throttle the gyroscope (keep highest power sensor off until needed)
- **Combine multiple sensors to improve sensing**
 - Pressure + GPS = faster GPS fix
 - Camera + Sensor Fusion = Augmented Reality
 - inElevator sensor?

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Comparison of Mobile OS Sensor Support

Sensor	iOS 5	Android	Win8
Accel/Mag/Gyro	✓	✓	✓
Pressure/Humidity	x	✓	x
Quaternion	CMAttitude	ROTATION_VECTOR	Orientation
Euler Angles	CMAttitude	ORIENTATION (depr.)	Inclinometer
Dynamic Acceleration	userAcceleration	LINEAR_ACCELERATION	Shake
Gravity in body frame	gravity	GRAVITY	Tilt
Tilt-compensated Compass	x	x	Compass
In Elevator	x	x	x

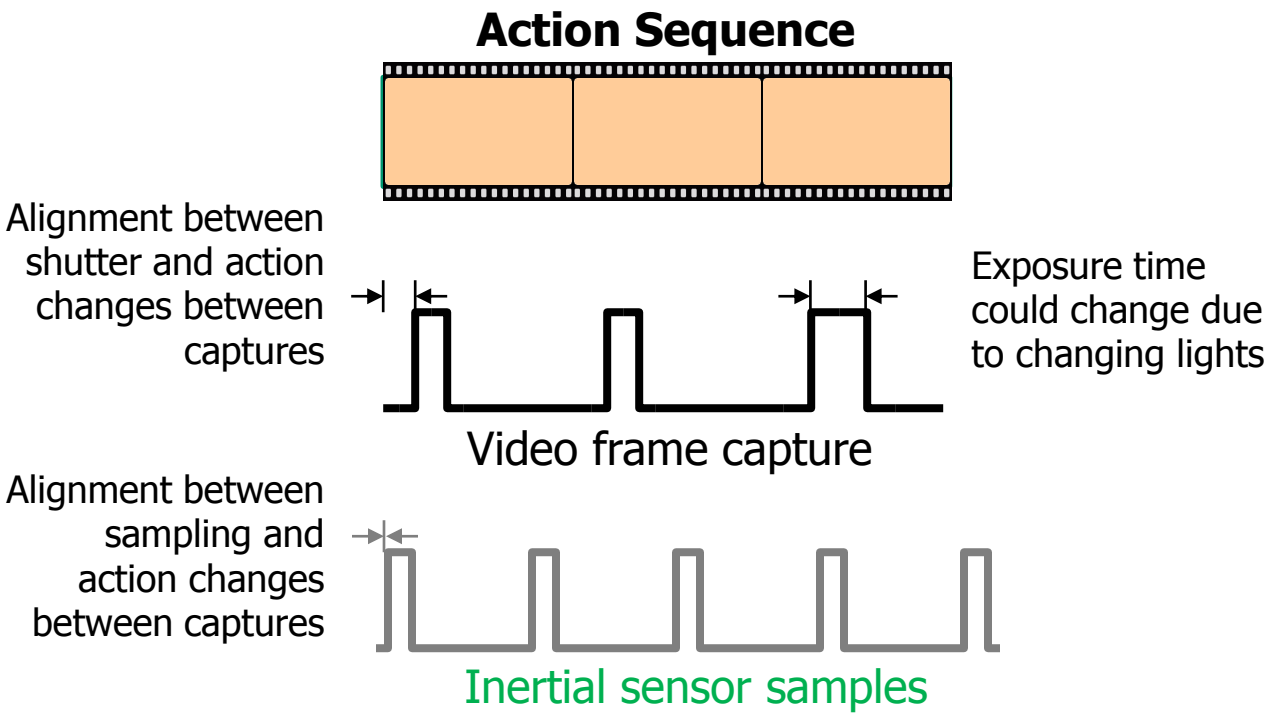
Virtual Sensors, e.g.



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Need Unified Timestamp between Sensors

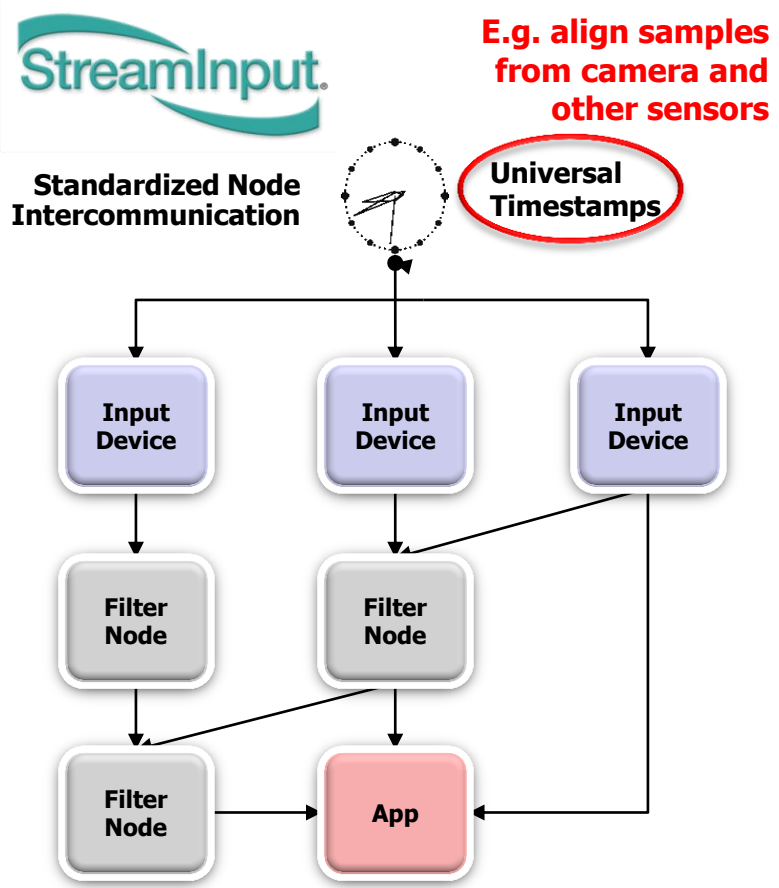
- **Sensors work on different time bases that drift**
- **Not all sensors support the same sampling rate**



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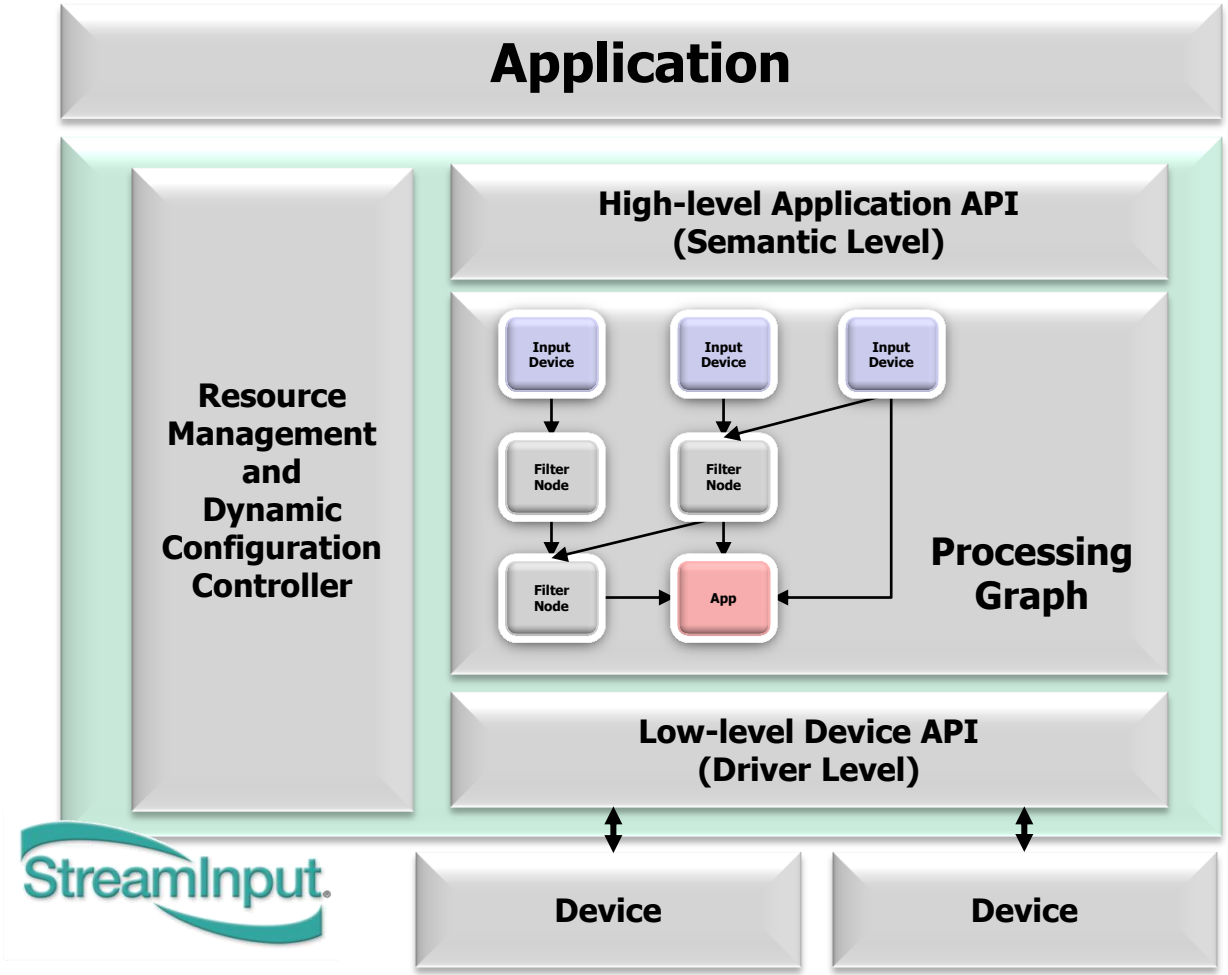
StreamInput Concepts

- **Standardized Application-defined filtering and conversion**
 - Can create virtual input devices
- **Sensor Hardware Vendor Agility for OEMs**
 - Allows standardized interface for hardware accelerated features
- **Extensibility to any sensor type**
 - Can define new node data types, state and methods
- **Sensor Synchronization**
 - Universal time stamp on every sample



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StreamInput Architecture



1. Setup Processing Graph (or use pre-supplied graph), request and receive semantic sensor stream through High-level API
2. Optionally, dynamically configure sensor processing through Low-level API – can tune power vs. performance

Implementable over existing OS input APIs to simplify adoption

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Sensor Platforms

- We create algorithms for sensors

- More information at our blog: www.sensorplatforms.com
- jsteele@sensorplatforms.com



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HOT CHIPS

The 11ers

Platform Performance

Dan Wexler, CxO The 11ers

HOT CHIPS

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Hot!

Sell More ^ Chips

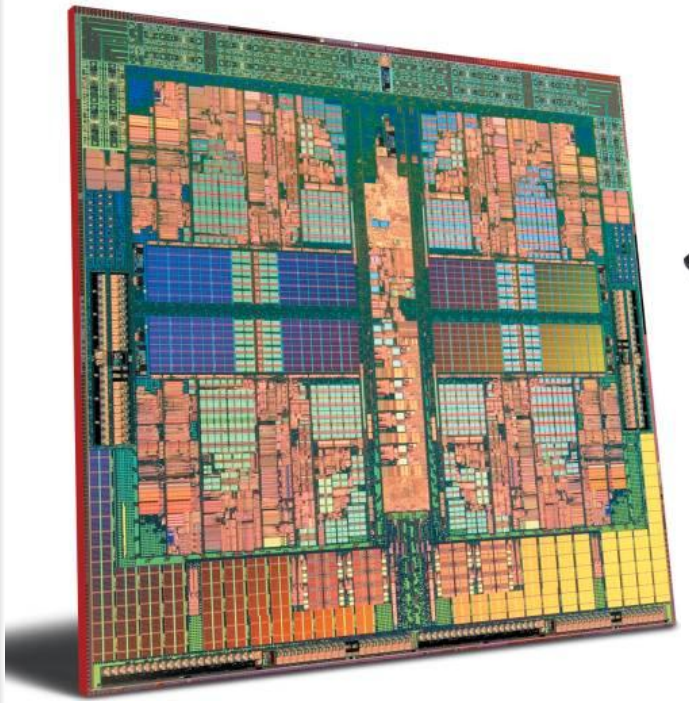


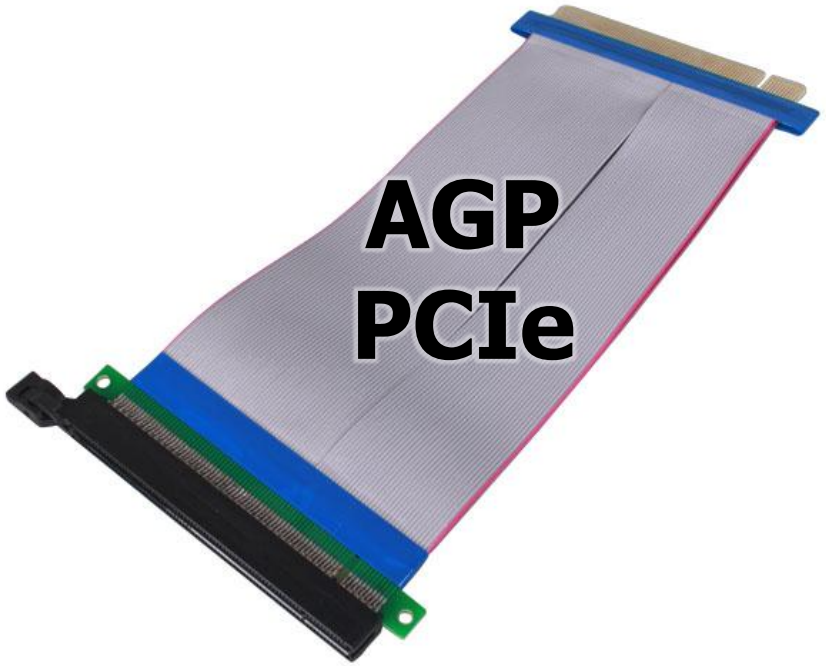


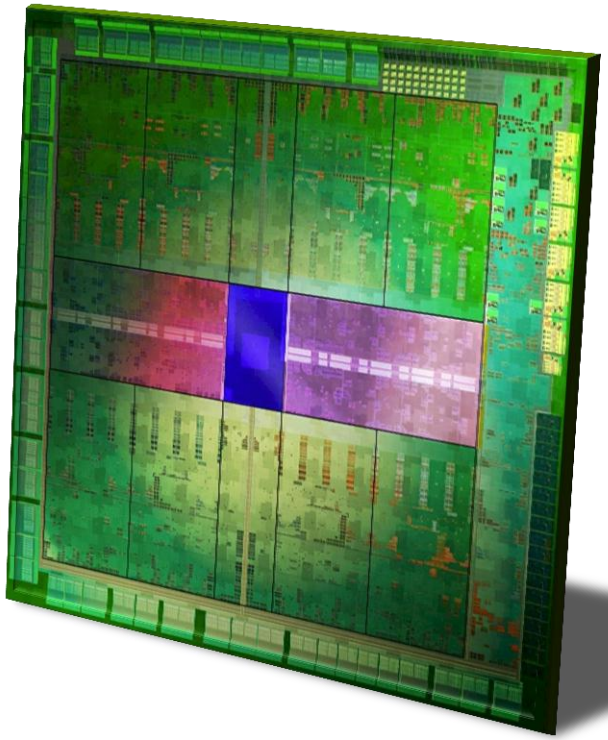


Prosumer Apps

CPU

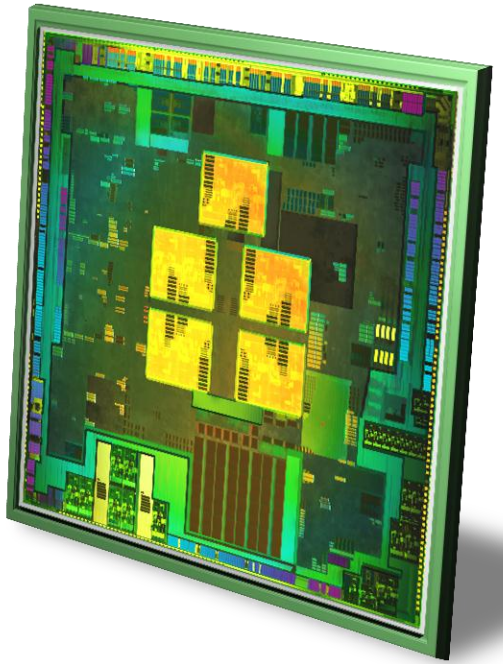


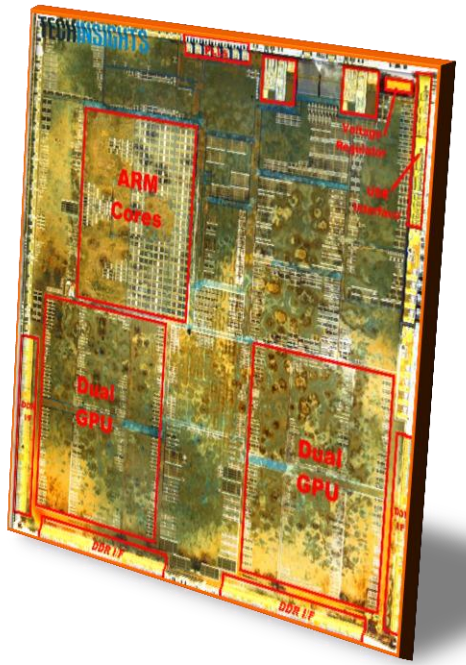


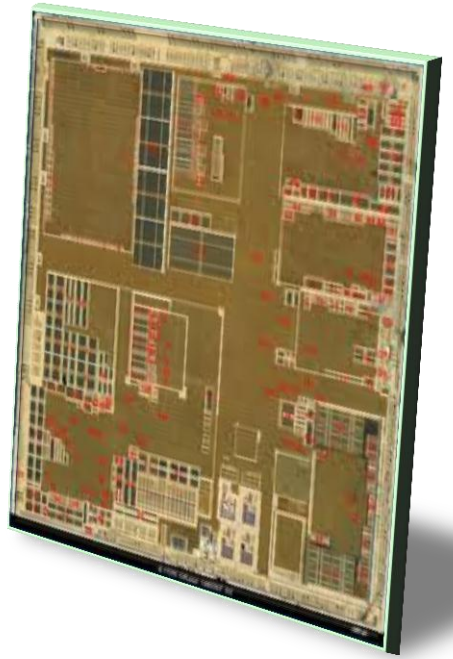


GPU

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Tegra **Apple** **Snapdragon**



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The 11ers

"Leading edge graphics in tasty mobile bytes."

Small Scope → Low Risk → Experience



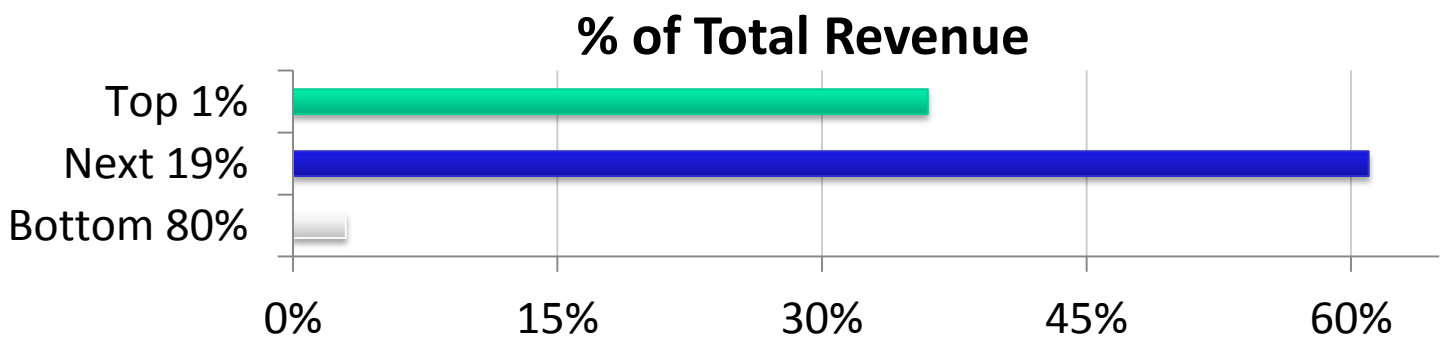
* http://DaveAddey.com/?p=893, 7/26/12

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$5B & 650K

Top 1% get 36% ($270K) | **Next 19% get 61% ($25K)** | **Last 80% get 3% ($290)**

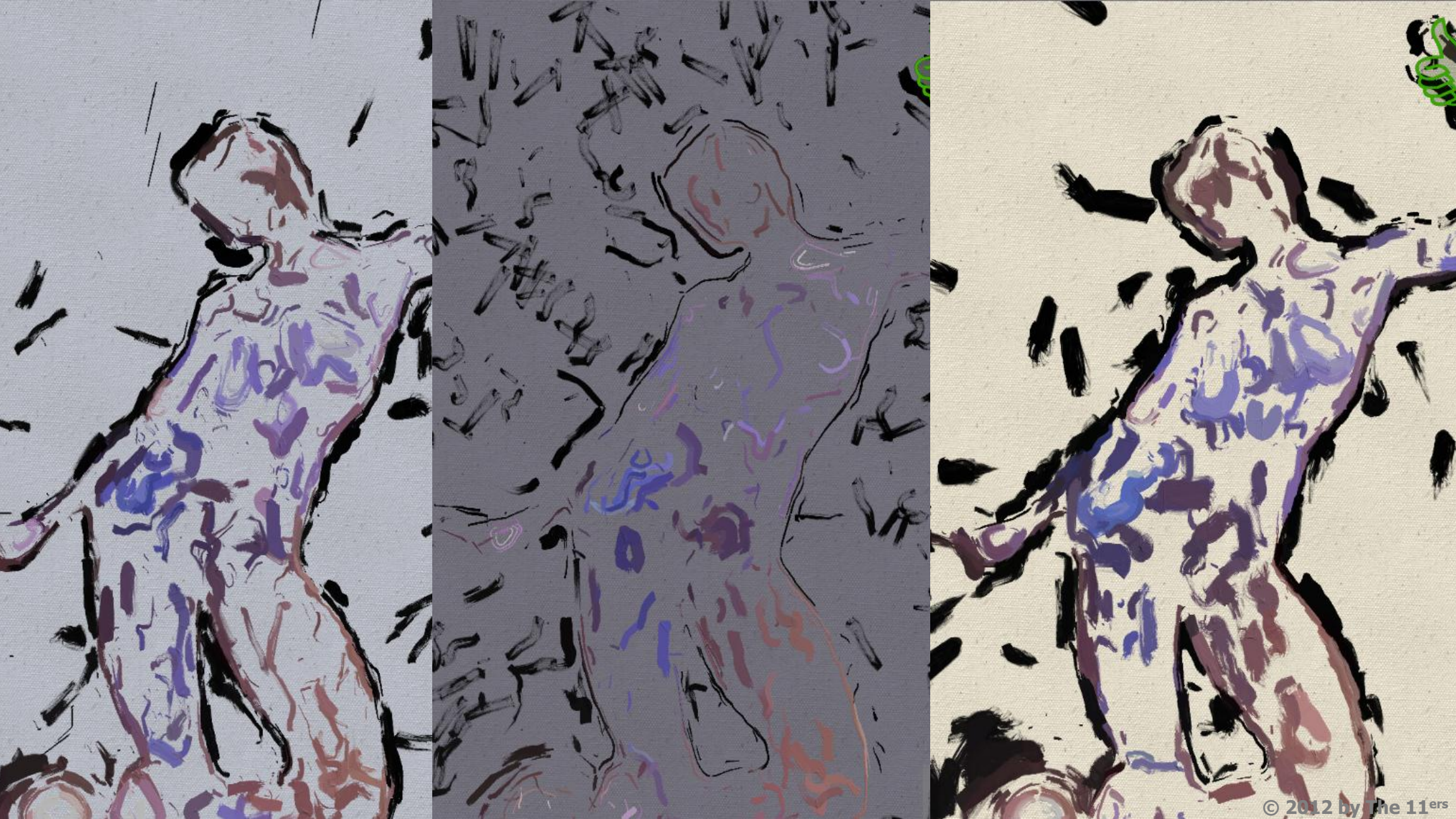
51 titles *before* Angry Birds



* http://DaveAddey.com/?p=893, 7/26/12


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Dynamic, Dependent, Reusable



No Vertex Texture! ☹ 5x Perf & TAM!

CPU

Face Detect

Stroke Geometry

GPU

Orient

Render

Difference

Shade







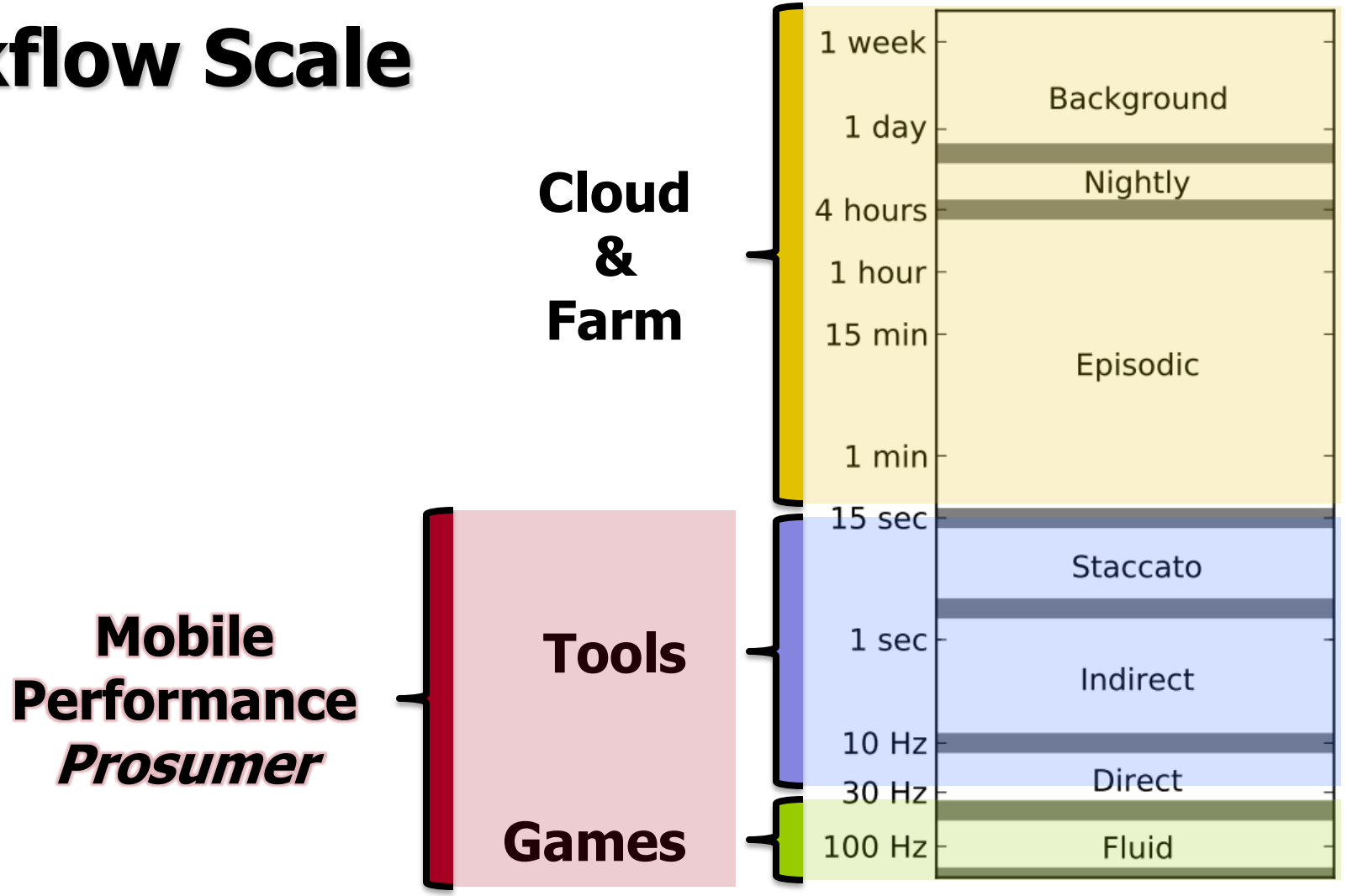


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Workflow Scale



Enderton & Wexler, "The Workflow Scale: Why 5x Faster Might Not Be Enough", CGI 2011

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What's Shared Memory?

- **No copies (OpenGL API forces copies)**
- **Simplified synchronization (map/unmap, fence, cache flush)**
- **Shared virtual address space (segmented ok)**
- **Texture instead of attributes? (Why VAR failed?)**
 Must be able to dynamically generate geometry on GPU and CPU (☺ GLES3)
- **Gosh, it would be really nice if pointers Just Worked ™**
- **Shared memory uses *less power & less bandwidth***







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Leapfrog Opportunity

- **We tried and failed for 10 years to move more algorithms to the GPU due to the lack of shared memory and the cost of bandwidth.**
- **Mobile UMA eliminates the bottleneck, fix the APIs and apps will follow.**
- **Shared memory is *lower power* → inevitable.**
- **Shared memory is *transformative* → whole new classes of apps.**

Thanks to Cass Everitt, Eric Enderton

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AFTERNOON TUTORIAL

	Die Stacking	
2:00 – 2:15	3-D Stacking Tutorial Introduction	Liam Madden, **Xilinx**
2:15 – 3:05	Foundry TSV Enablement For 2.5D/3D Chip Stacking	Remi Yu, **UMC**
	Full Processing Interposer Process	Choon Lee, **Amkor**
3:05 – 3:55	Roadmap for Design and EDA Infrastructure for 3D Products	Riko Radojcic, **Qualcomm**
	Xilinx SSI Technology Concept to Silicon Development Overview	Shankar Lakka, **Xilinx**
3:55 – 4:10	**Break**	
4:10 – 5:00	Memory Consideration and Heterogeneous Die	Bryan Black, **AMD**
	Optical Backplanes with 3D Integrated Photonics?	Ephrem Wu, **Xilinx**
5:00 – 5:30	Panel	
5:30 – 7:00	**Reception**	

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Die Stacking

2.5D/3D die stacking increases aggregate inter-chip bandwidth and shrinks board footprint while reducing I/O latency and energy consumption. By integrating in one package multiple tightly-coupled semiconductor dice – each possibly in a process optimized for power, performance and costs for a particular function – this technology gives system designers additional options to partition and scale solutions efficiently. Die stacking has already transformed the design of high-end CMOS image sensors, and it promises to also enhance FPGA, graphics and mobile applications.

In Part 1 of this tutorial we will examine the key enabling technologies such as silicon interposer, TSV, micro-bump and assembly integration. In Part 2 we will cover the design considerations & trade-offs of 2.5D/3D in CAD, ESD and architecture. Part 3 will showcase how the technology is used in systems and applications for memory integration, optics integration and monolithic die partitioning.
Schedule

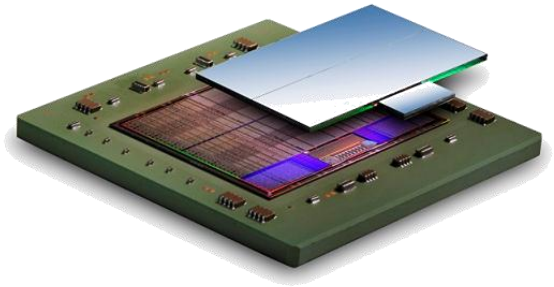
2:00pm – 2:15pm: Introduction by Liam Madden from Xilinx
2:15pm – 3:05pm: Technology
Fab, Interposer and TSV by Remi Yu from UMC
Assembly and Micro Bumps by Choon Lee from Amkor
3:05pm – 3:55pm: Design Considerations
3D, CAD and Floorplanning by Riko Radojcic from Qualcomm
2.5D, CAD and ESD by Shankar Lakka from Xilinx
3:55pm – 4:10pm: Break for refreshments
4:10pm – 5:00pm: System Implications
Memory Consideration and Heterogeneous Die by Bryan Black from AMD
Optical Considerations by Ephrem Wu from Xilinx
5:00pm – 5:30pm: Panel moderated by Liam featuring all the speakers

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3-D Stacking Tutorial
Introduction

AMD Amkor Technology QUALCOMM UMC XILINX

Liam Madden
Corporate Vice President
Xilinx
Aug 27th 2012



Dedicated to the Memory of Chuck Moore: Visionary



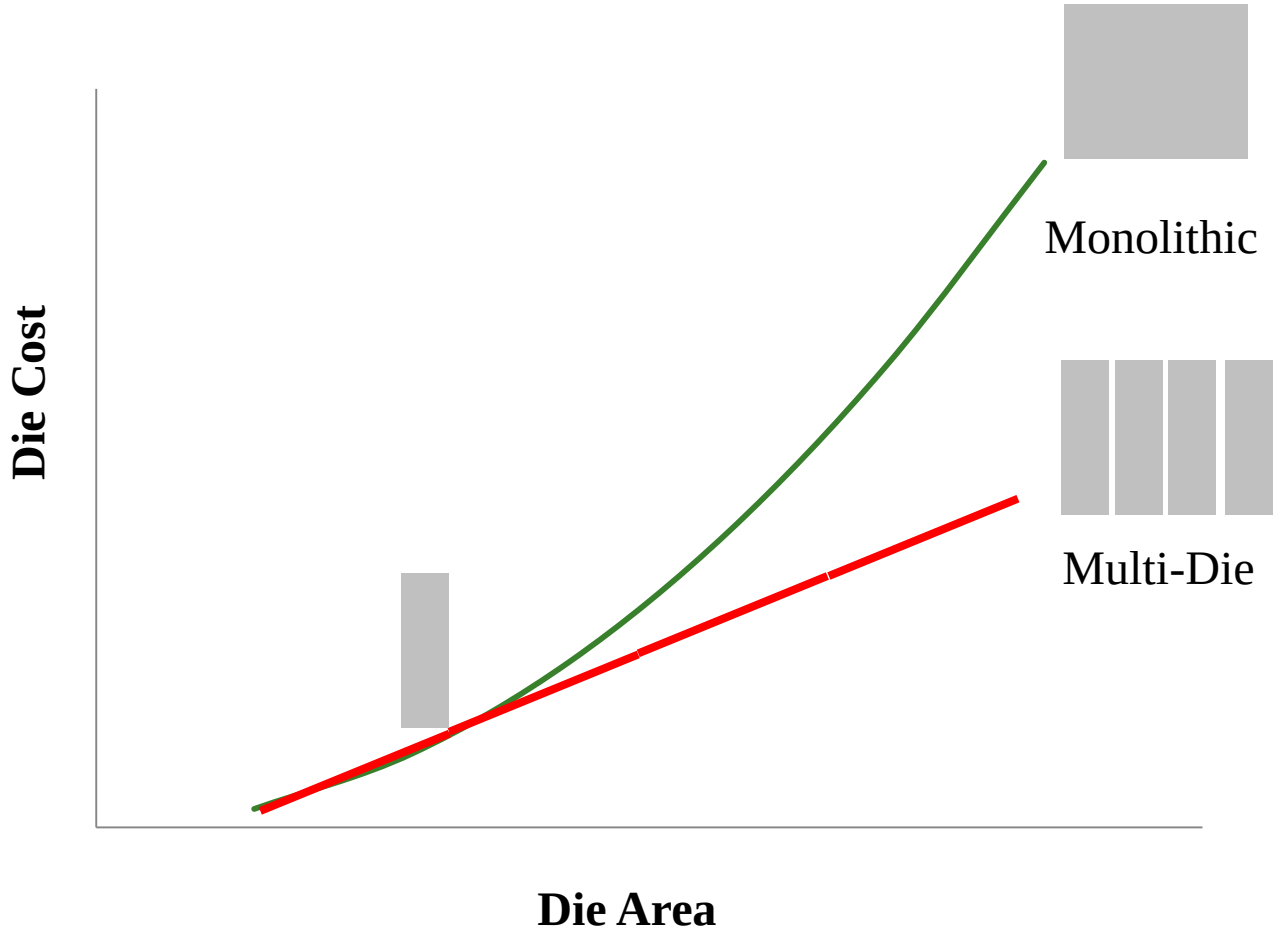
Chuck Moore,
AMD Corporate Fellow
1961-2012

Agenda

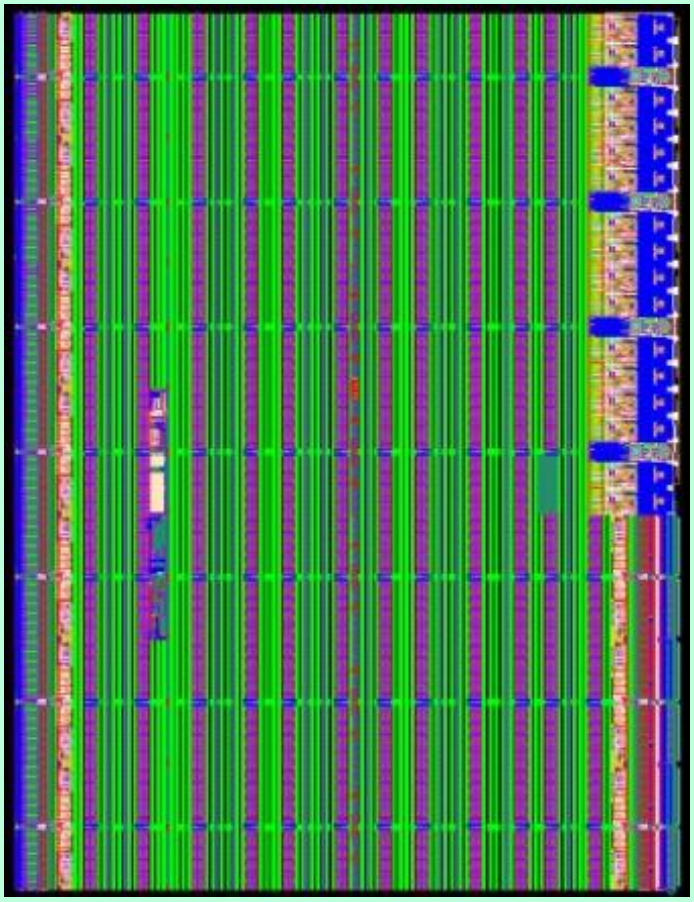
- Introduction: Liam Madden, Corp VP, Xilinx (2:00-2:15)
- Technology: (2:15-3:05)
 - Foundry: Remi Yu, Director Marketing, UMC
 - OSAT: ChoonHeung Lee, Corp VP, Amkor
- Design Considerations: (3:05-3:55)
 - Mobile Communications: Riko Radojcic, Director, Qualcomm
 - FPGA: Shankar Lakka, Director Integration, Xilinx
- Break (3:55-4:10)
- System Implications (4:10-5:00)
 - Processor and GPU: Bryan Black, Senior Fellow, AMD
 - Integrated Optics, Ephrem Wu, Senior Director, Xilinx
- 5:00-5.30 Panel Discussion

Cost Comparison: Monolithic vs Multi-Die

"Moore's Law is really about economics" *Gordon Moore*



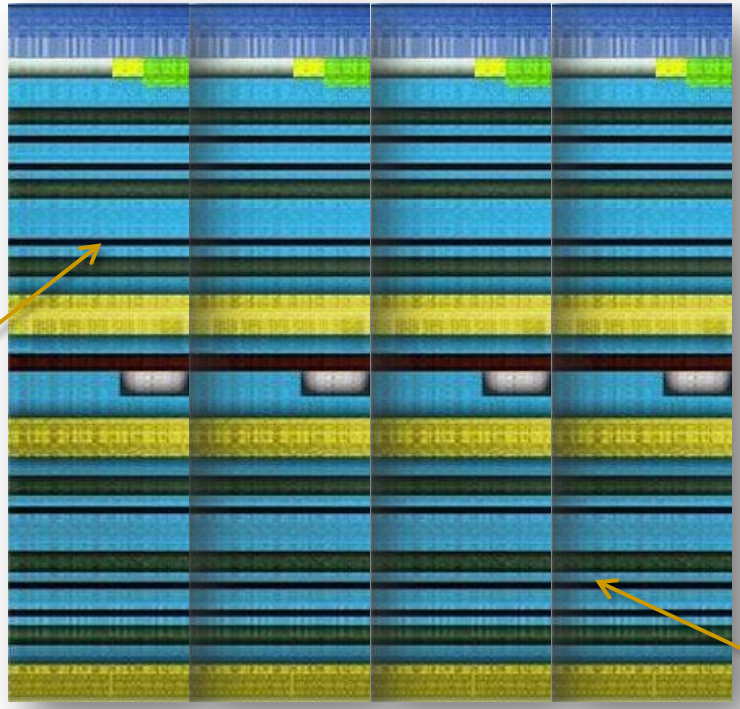
Why is first 3D logic product an FPGA?



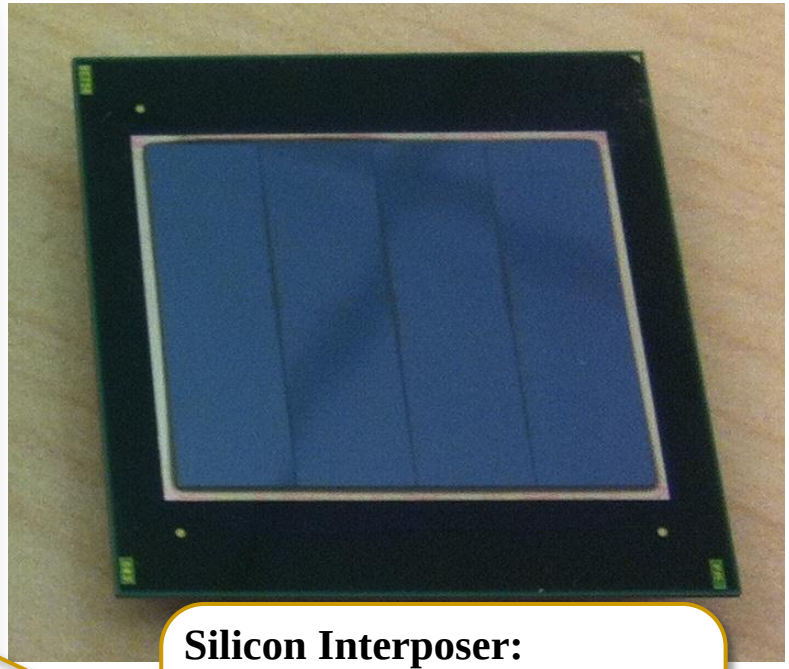
- Natural partition using “long lines”
- Very low “opportunity cost”
- No 3rd party dependence
- “Size matters” to customers
- Compelling value proposition “next generation density in this generation technology”

Virtex 2000T: Homogeneous Stacked Silicon Interconnect Technology (SSIT)

FPGA slice



FPGA Slices Side-by-Side

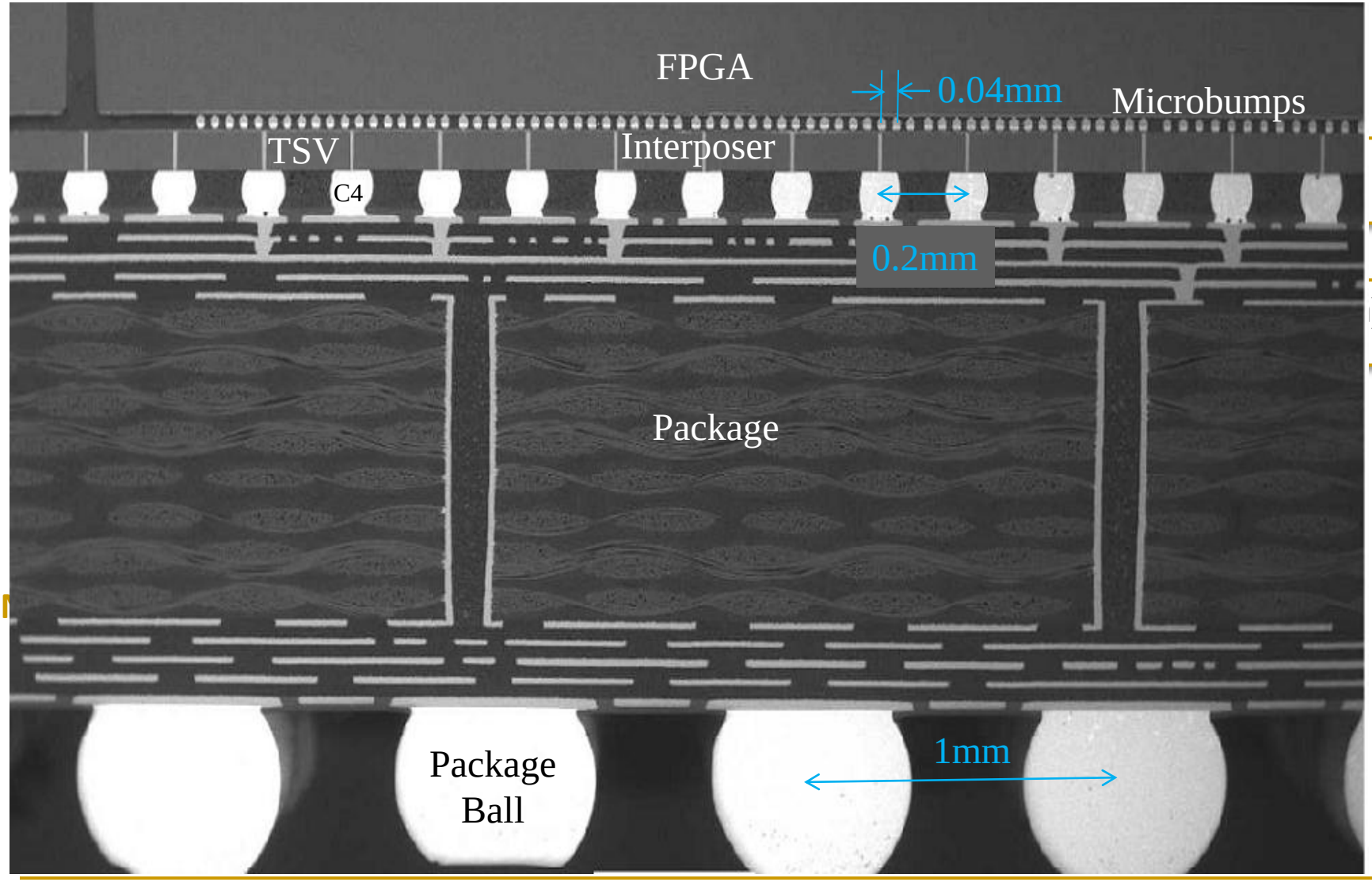


Silicon Interposer:

>10K routing connections between slices

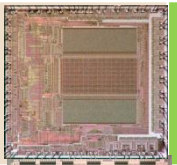
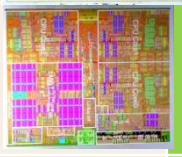
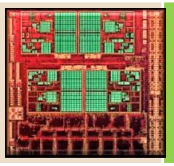
~1ns latency

Elements of SSIT



3 Decades of Microprocessor Integration: A personal history

"Integrate or be integrated" *Fred Webber, former CTO AMD*

Year	Company	Product		Integration Level						
				Core				L2$	North Bridge	GPU
				DP	Ctl	L1 $	FPU			
1983	Harris	J11	4um 							
1989	DEC	Rigel	1.5um 							
1991	DEC	Alpha	0.75um 							
2005	Microsoft	Xenon	90nm 	3 Core						
2011	AMD	Fusion	40nm 	2 Core						

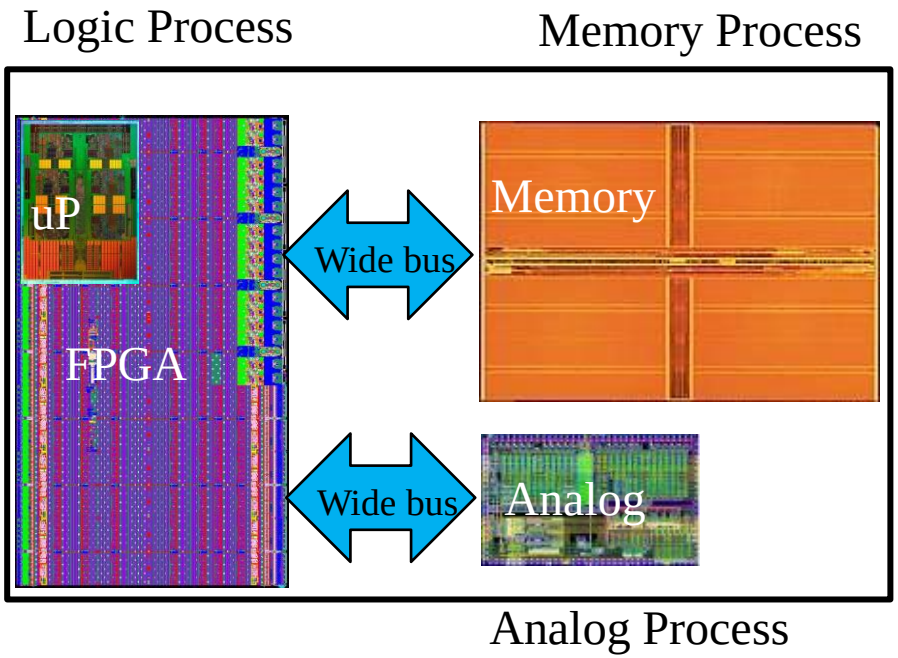
STACKONOMICS

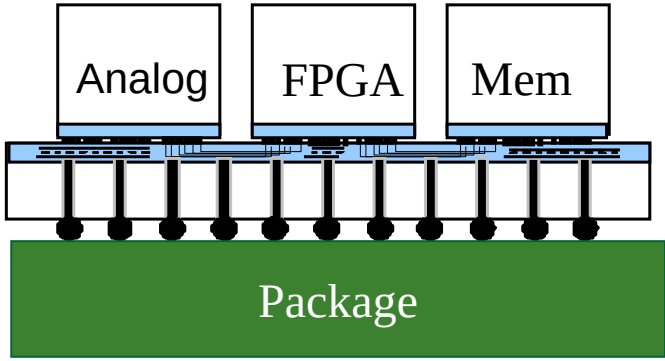


What happened to System on a Chip?

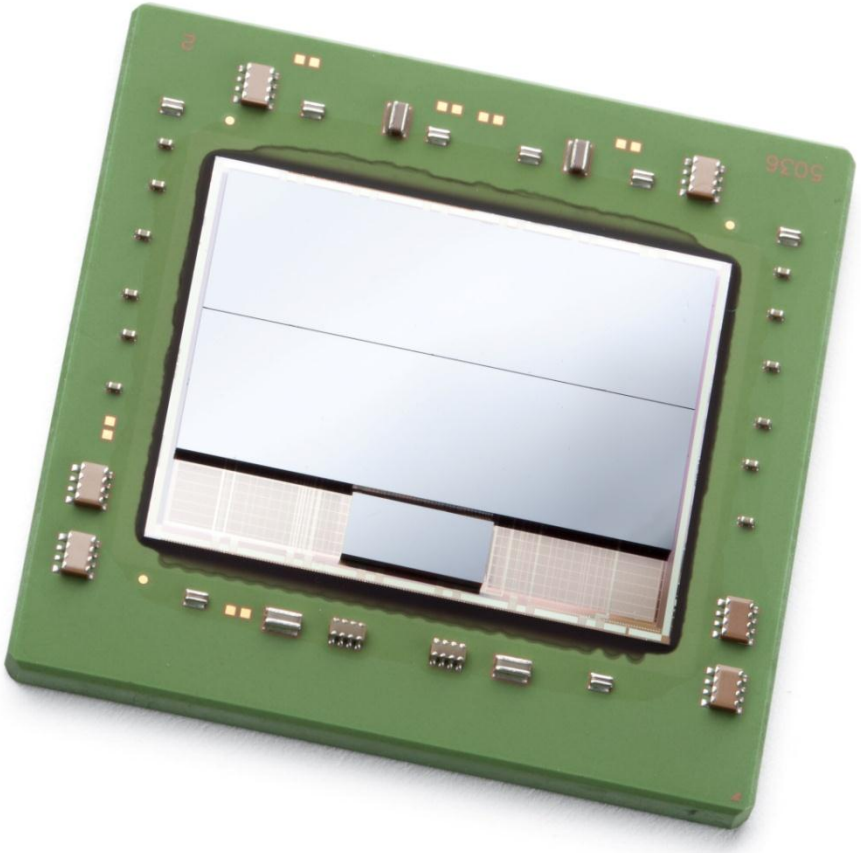
	Logic	Memory	Analog
Global Revenue 2011	$150B	$68B	$45B
Moore Scaling	Good (except I/O)	Good (except I/O)	Poor
Technology "Vintage"	2012	2012	2000
Transistor Characteristics	High performance/ Low leakage	Low leakage/ moderate performance	Stable with good voltage headroom
Metallization	>9 layers	<5 layers	<6 layers
Differentiators	High density logic	Charge storage	Passives, Optical

Crossing the packaging chasm

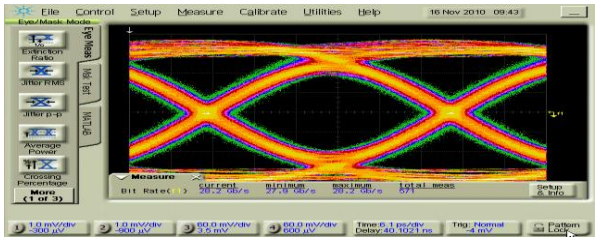




7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die



Virtex-7 HT @ 28Gbps



Foundry TSV Enablement For 2.5D/3D Chip Stacking

Remi Yu, UMC

Hot Chips 24

August 27, 2012

UMC

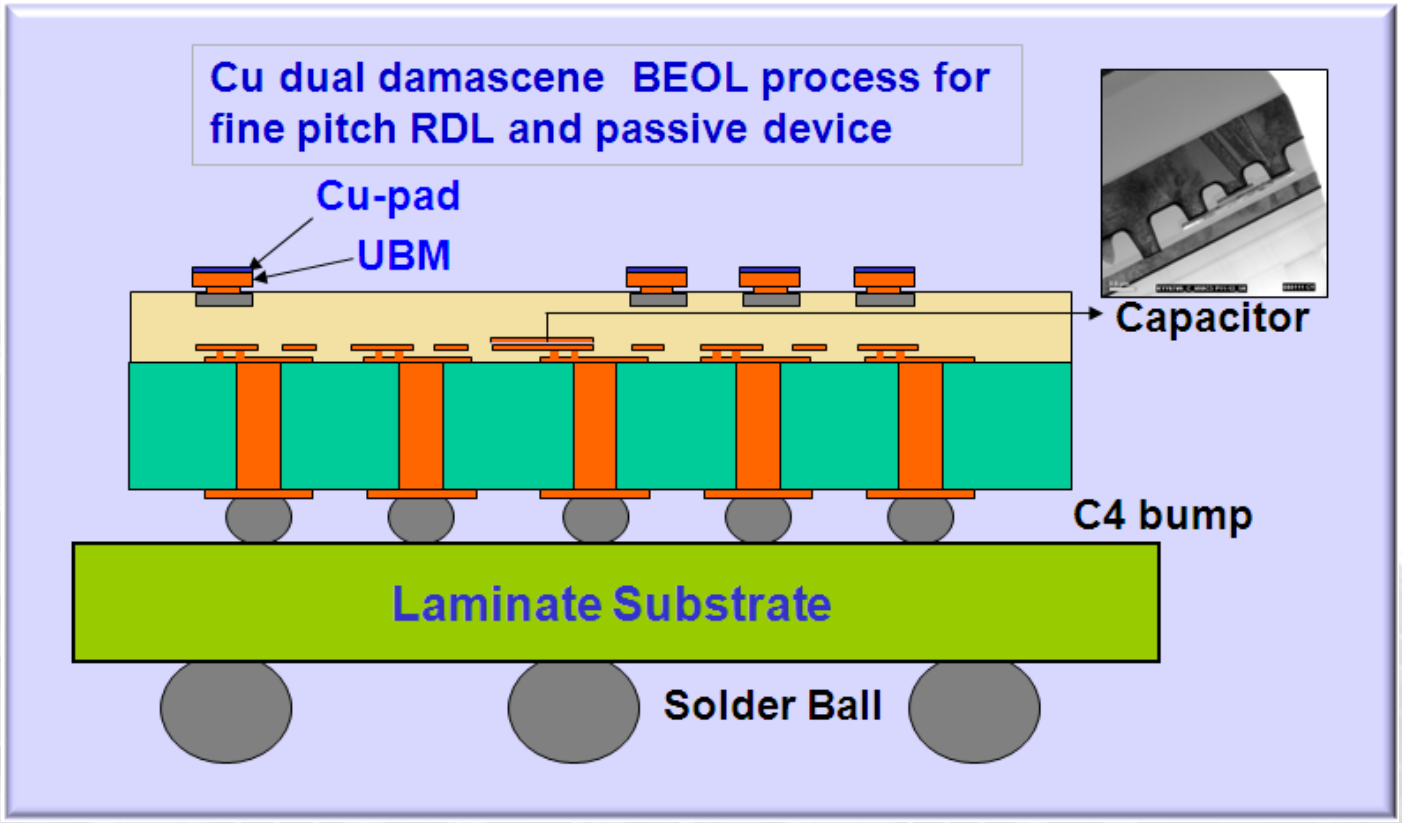
Customer-Driven Foundry Solutions

Outline

- 2.5D/3D Applications
- Foundry TSV Enablement
- Ecosystem Work Flow
- Summary

2.5D/3D Applications

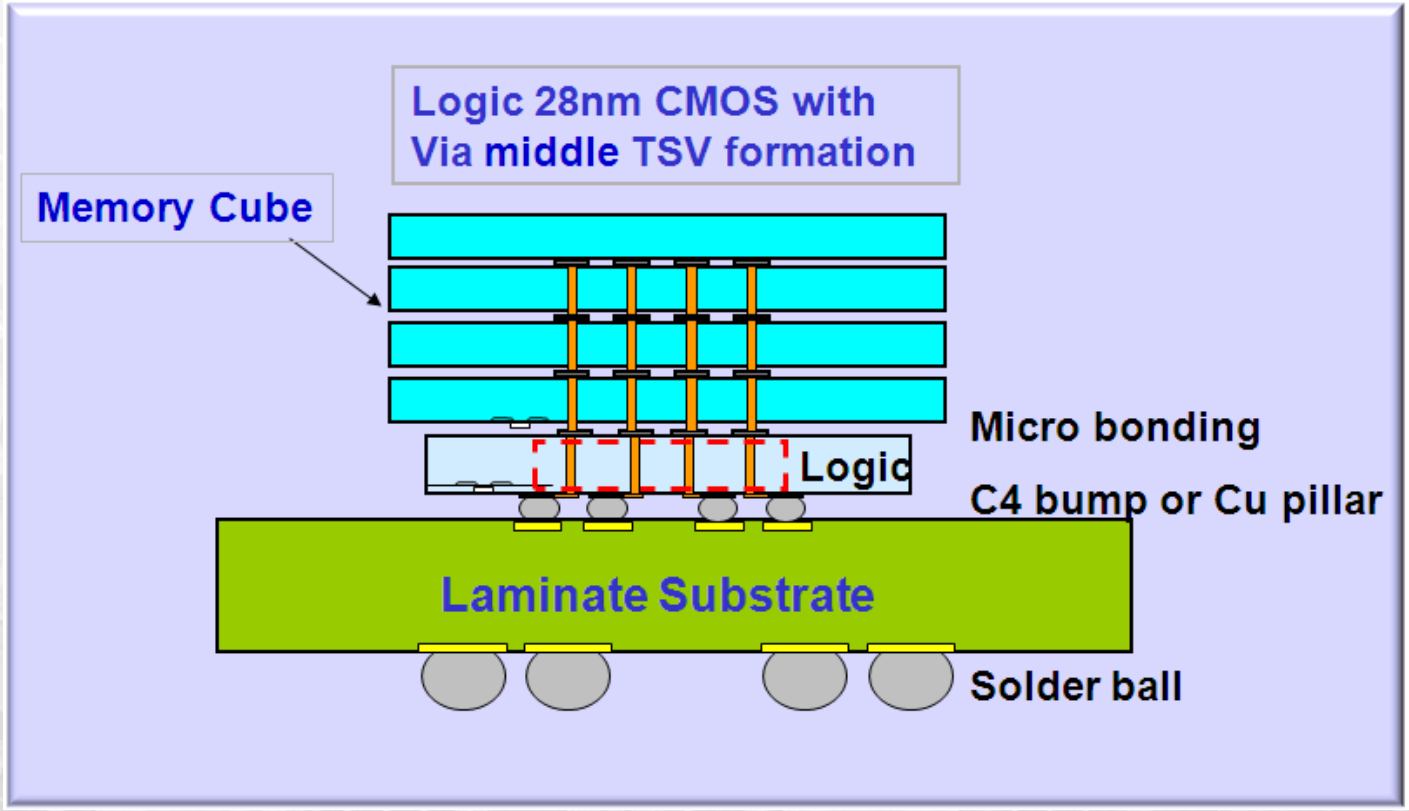
2.5D Si Interposer Stacking



- Logic/logic: FPGA, networking infrastructure
- Logic/memory: Gaming, HPC

3D Logic/Memory Stacking

- Via-Middle TSV 28nm Logic + Memory Cube

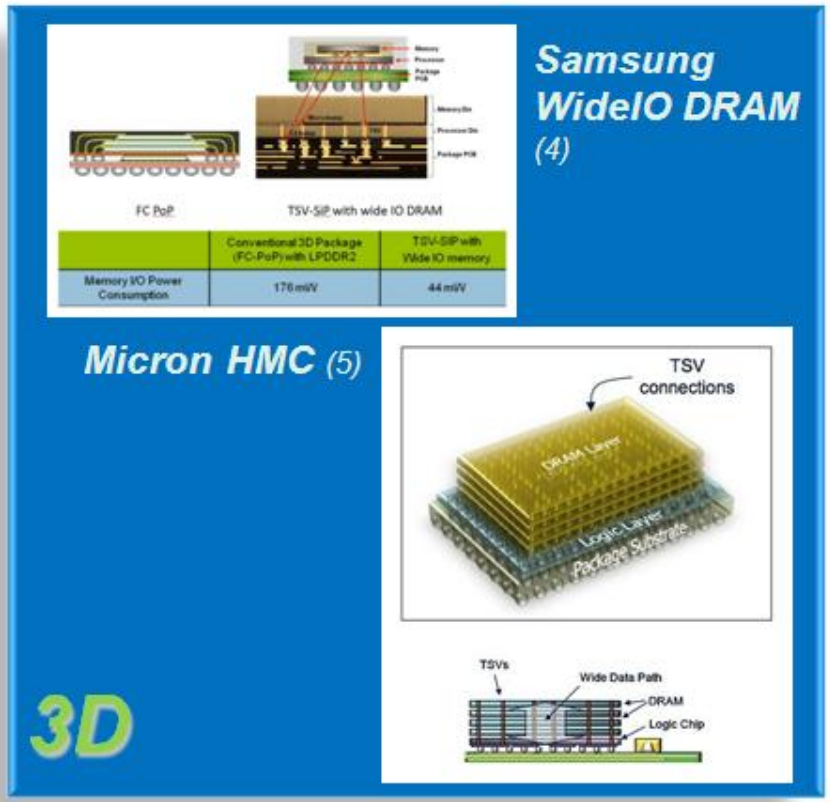


- Mobile WideIO, Computing WideIO, HMC

Application Examples

- More are being developed





(1) http://low-powerdesign.com/sleibson/2011/10/25/generation-jumping-2-5d-xilinx-virtex-7-2000t-fpga-delivers-1954560-logic-cells-consumes-only-20w/

(2) http://eda360insider.wordpress.com/2012/06/01/friday-video-3d-thursday-xilinx-virtex-7-h580t-uses-3d-assembly-to-merge-28gbps-xceivers-fpga-fabric/

(3) eSilicon, "GSA 3D Working Group", July 2012

(4) http://www.ecnmag.com/news/2011/03/samsung-wide-io-memory-mobile-products-deeper-look

(5) http://denalimemoryreport.com/2012/06/28/arm-hp-and-sk-hynix-join-hybrid-memory-cube-consortium-hmcc-first-spec-due-by-end-of-year/

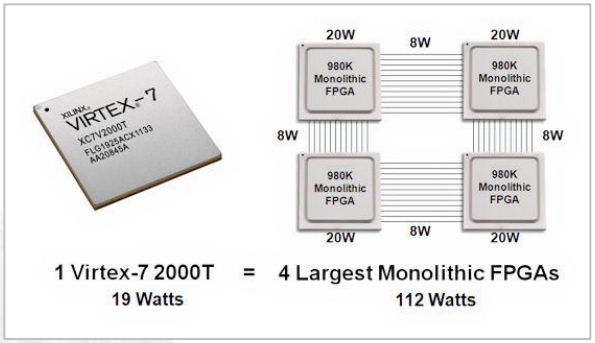
Cost-of-Ownership Advantages

Motivations:

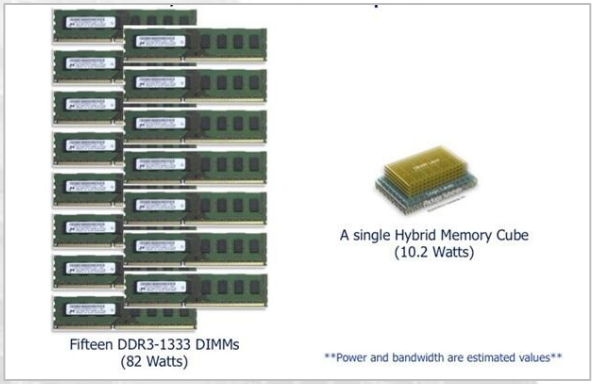
- Higher BW, lower W/BW, smaller form-factor

Opportunity of return on 3D IC investment:

- Chip process node optimization
 - Homogeneous partition
 - Cross-node combinations
- BOM cost optimization
 - Less demanding substrate/PCB, lighter cooling assembly, ...
- Ultimately: better product, better margin



Xilinx Virtex 7 *(1)*



Micron HMC *(2)*

(1) http://low-powerdesign.com/sleibson/2011/10/25/ generation-jumping-2-5d-xilinx-virtex-7-2000t-fpga-delivers-1954560-logic-cells-consumes-only-20w/

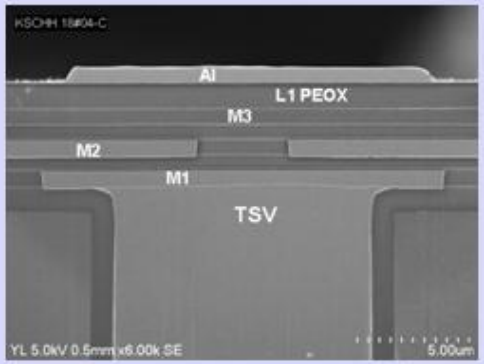
(2) http://www.i-micronews.com/news/Micron-Samsung-TSV-stacked-memory-collaboration-closer-look,7766.html

Foundry TSV Enablement

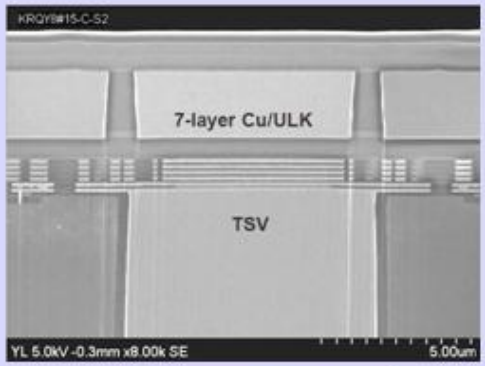
UMC

Customer-Driven Foundry Solutions

Foundry TSV Process Technology



Si Interposer

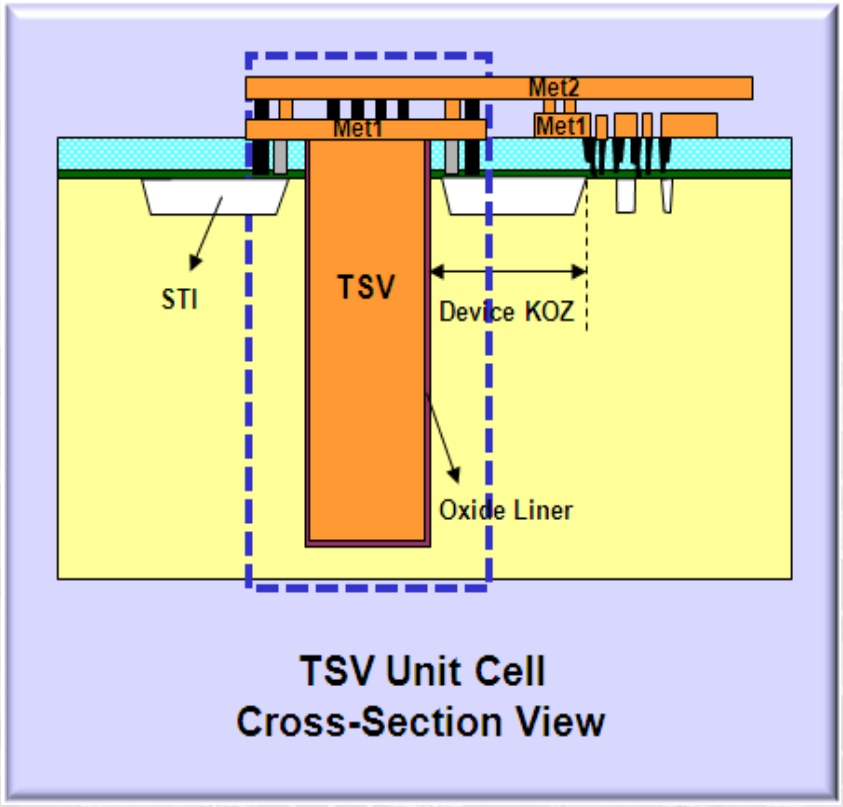


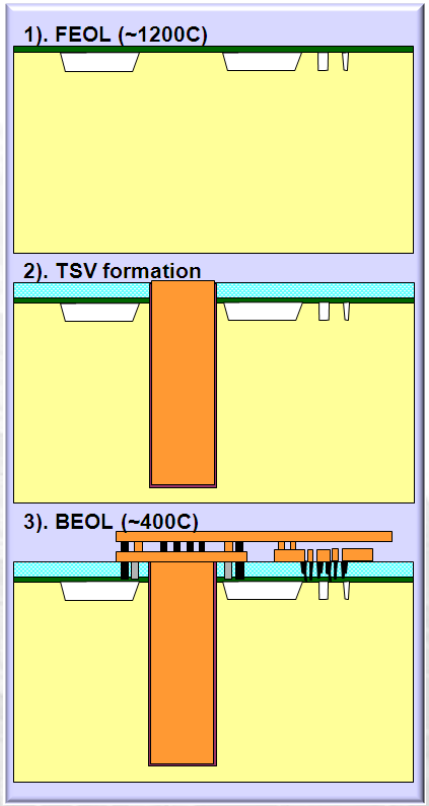
28nm 3D IC

- Mainstream: Via-middle Cu TSV
 - 2.5D: 65nm-generation BEOL
 - 3D: 28nm CMOS logic
- After 28nm entry, TSV for 3D may come as a standard option for foundry CMOS logic at 20nm and beyond

Example TSV Unit Cell

- Via-Middle TSV for 3D

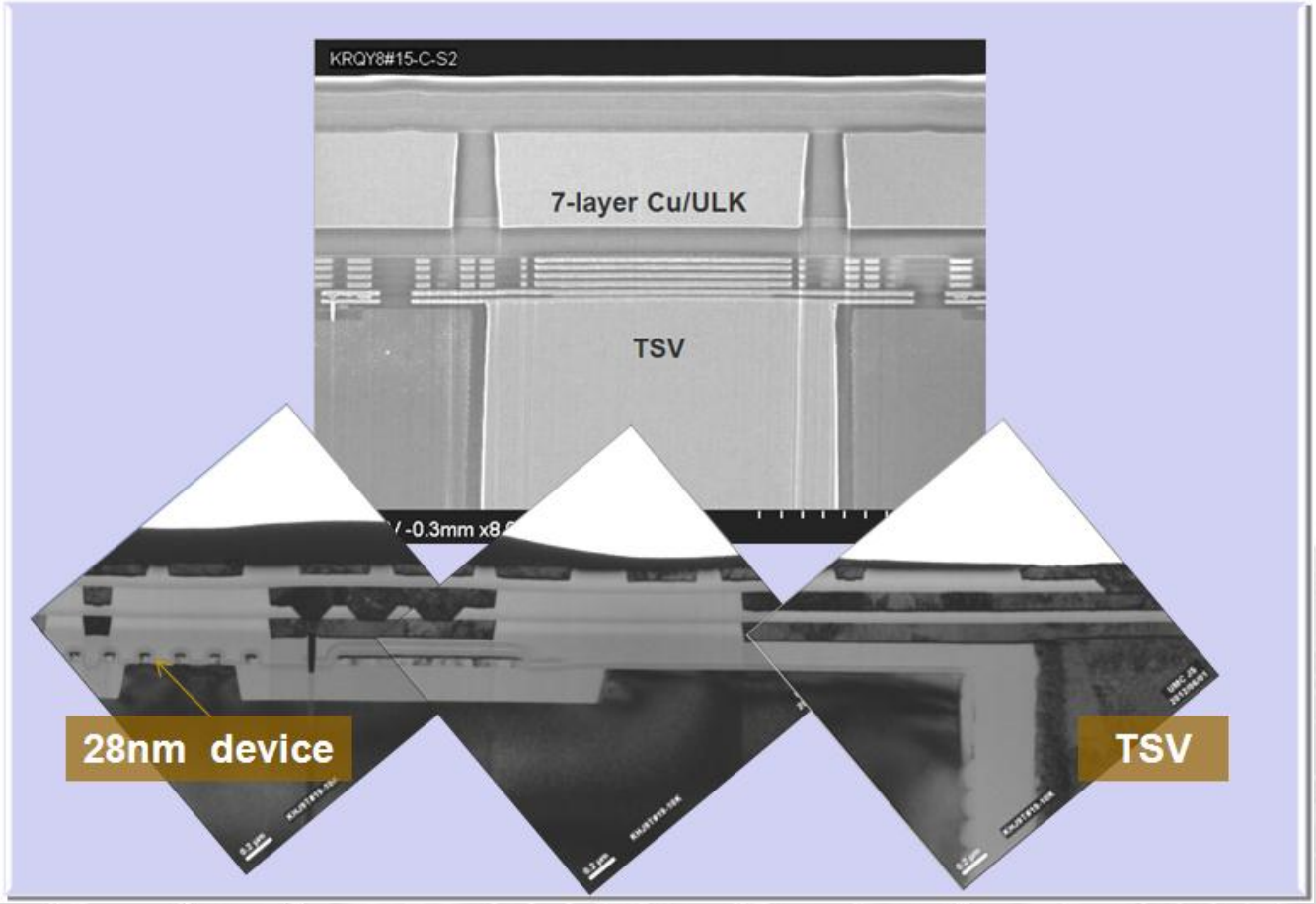




(drawn not to scale)

- TSV formed after CMOS, before contact/metal

UMC 28nm 3D IC



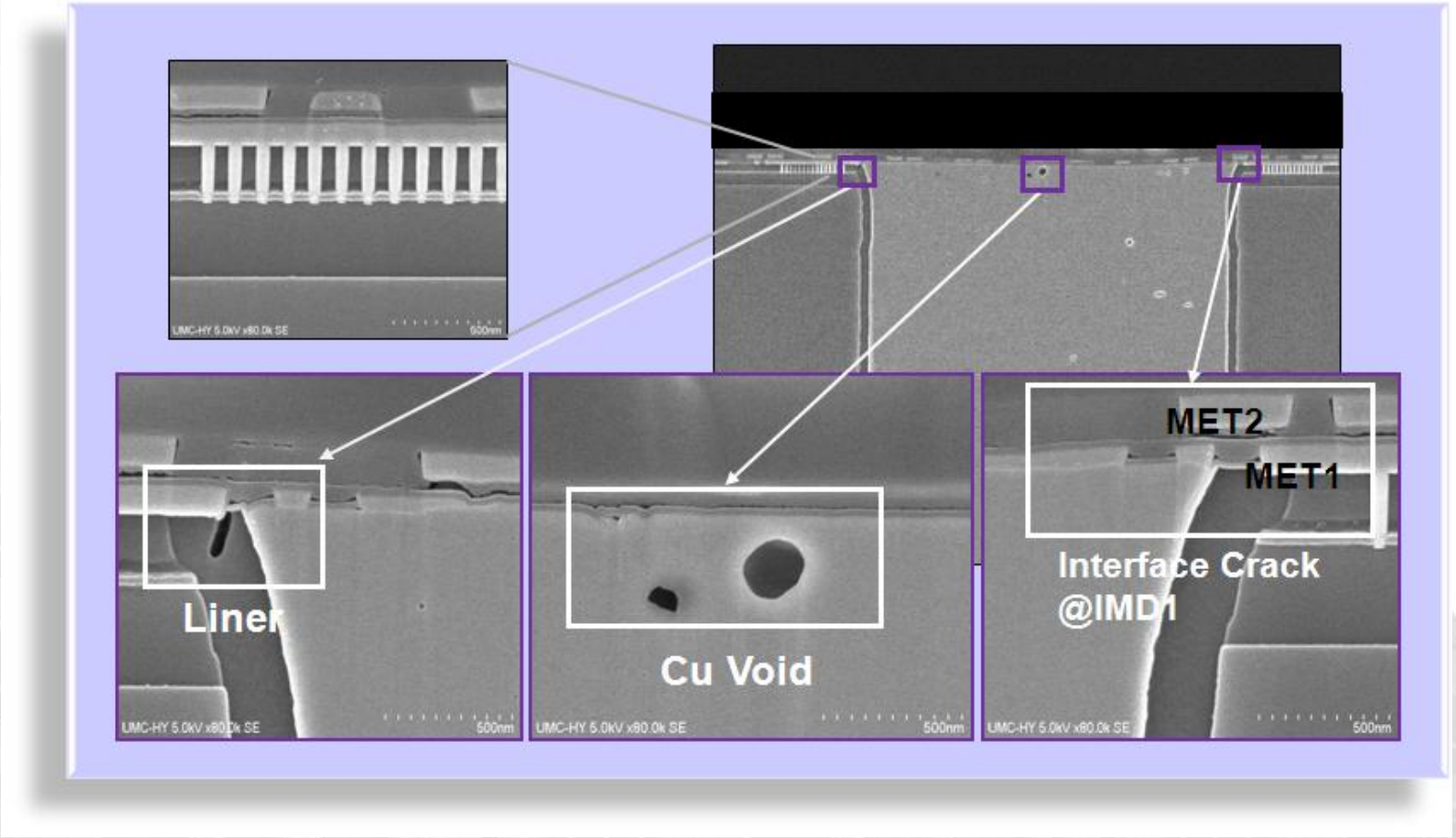
(CMOS device and TSV in proportion)

UMC Via-Middle TSV Unit Process



- Leveraging existing CMOS tools and capability
- Size is new to fab practice: diameter/depth

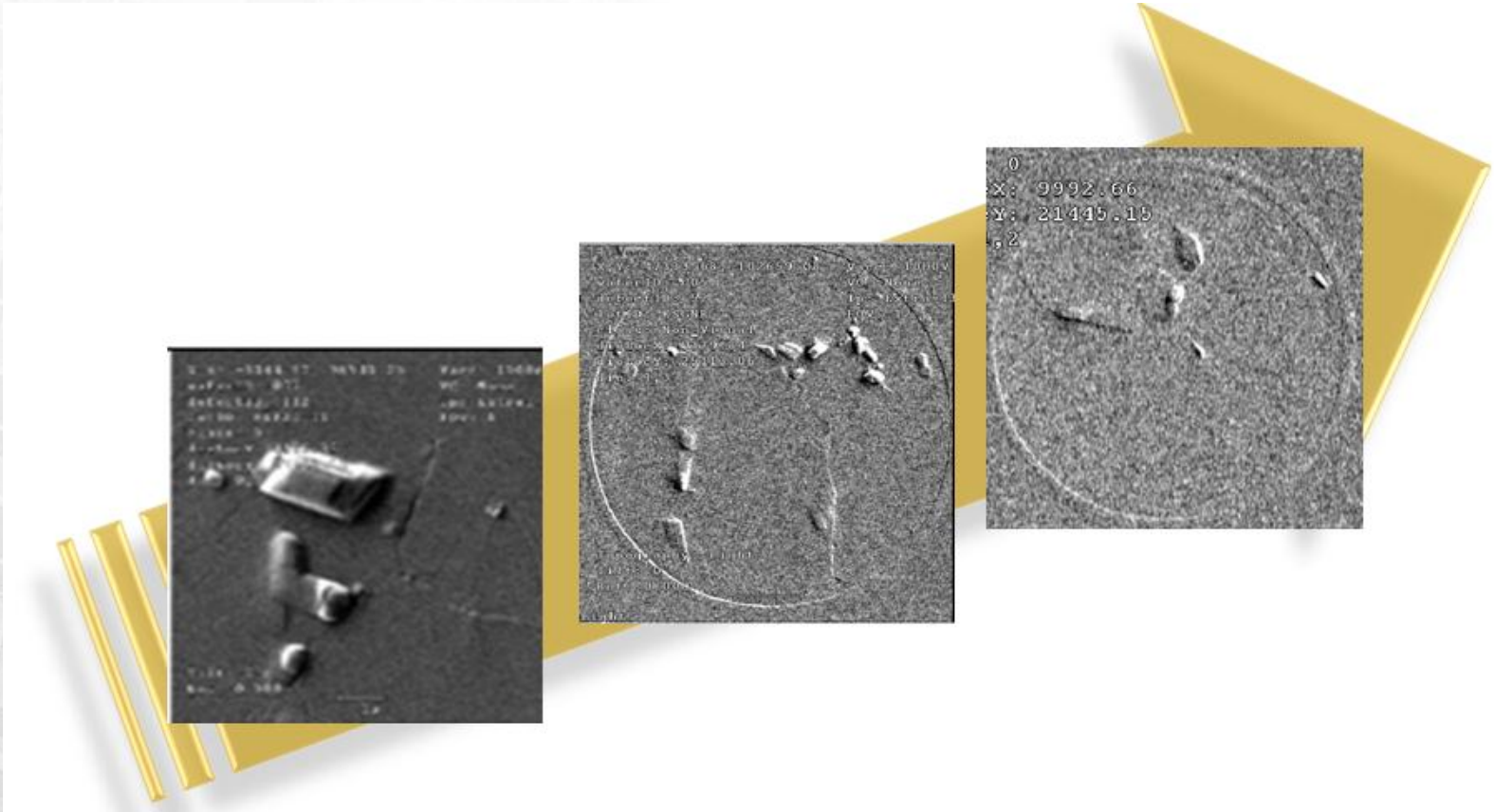
Early Stage TSV Process Issues



- TSV integrity – Cu fill, oxide liner, metal stack

ECP Cu Fill Process Optimization

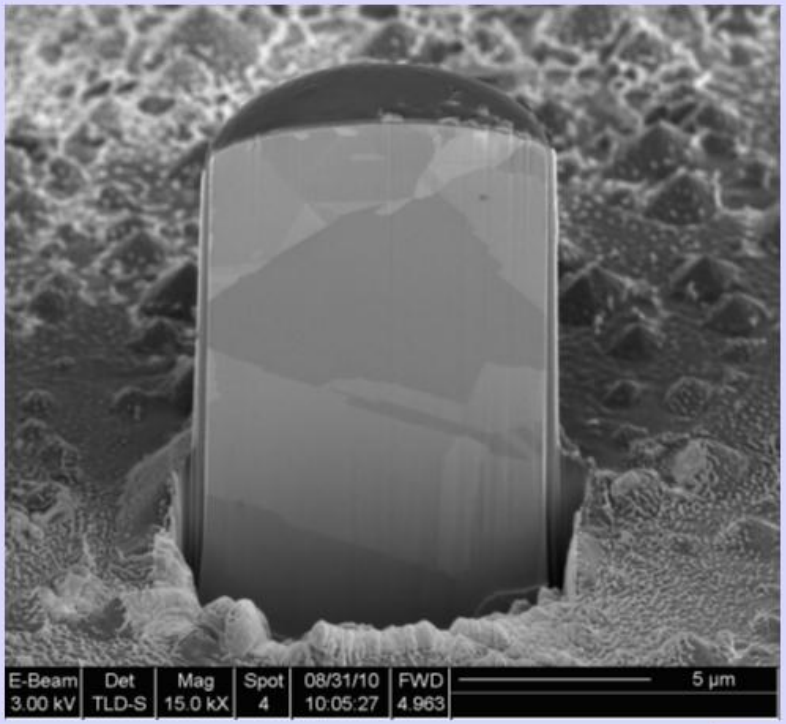
- Cu pumping reduction



- ECP Cu plating critical to TSV integrity

UMC Via-Middle TSV Solution

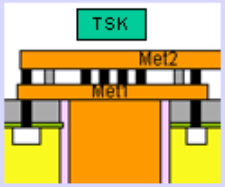
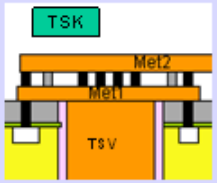
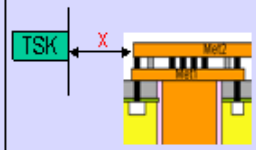




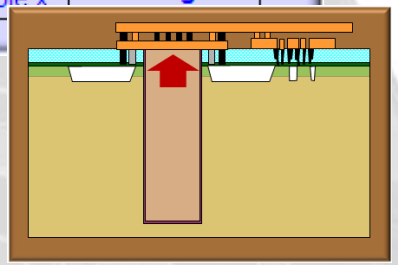
UMC via-middle TSV: void-free Cu gap fill

TSV Top Side Impact Evaluation

- BEOL WAT testkeys

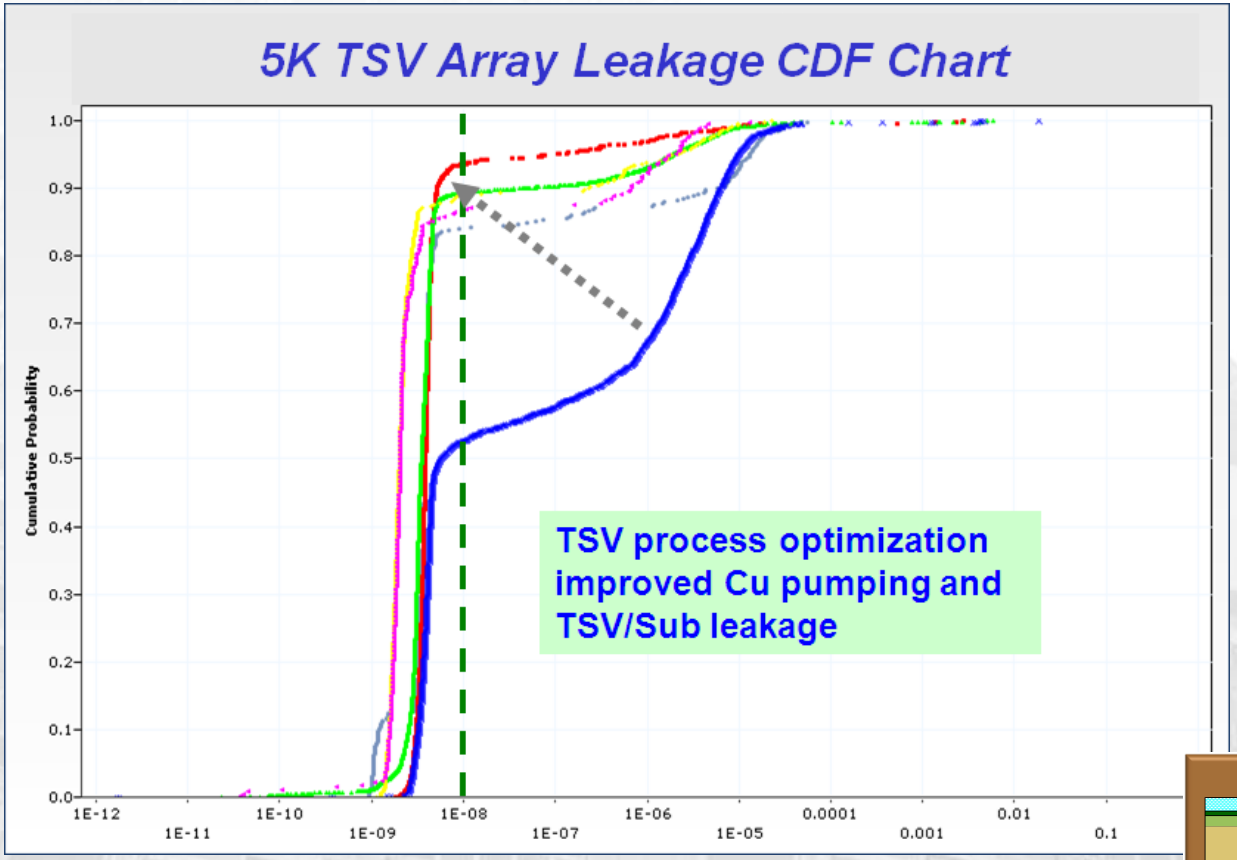
WAT test item	Layer	Testkey rule (w/s)	Above TSV	Cross TSV	Beside TSV	After Sinter
						
Metal Bridge	M3	1x W /1x S	Passed	Passed	Passed (min. x=1)	No significant change
		2x W /2x S	Passed	Passed	n/a	
	M4	1x W /1x S	Passed	Passed	Passed (min. x=1)	
		2x W /2x S	Passed	Passed	n/a	
Metal Resistance	M3	1x W /1x S	Passed	Passed	Comparable for variable x	No significant change
		2x W /2x S	Passed	Passed	n/a	
	M4	1x W /1x S	Passed	Passed	Comparable for variable x	
		2x W /2x S	Passed	Passed	n/a	
Via Bridge	V3	Com_run Via	Passed	Passed	Comparable for variable x	No significant change
		Non_com Via	Passed	Passed	Comparable for variable x	

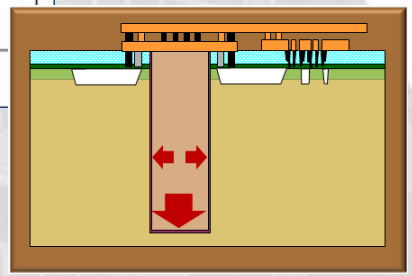
- Routing over TSV allowed



TSV Bottom Side Impact Evaluation

- Leakage CDF

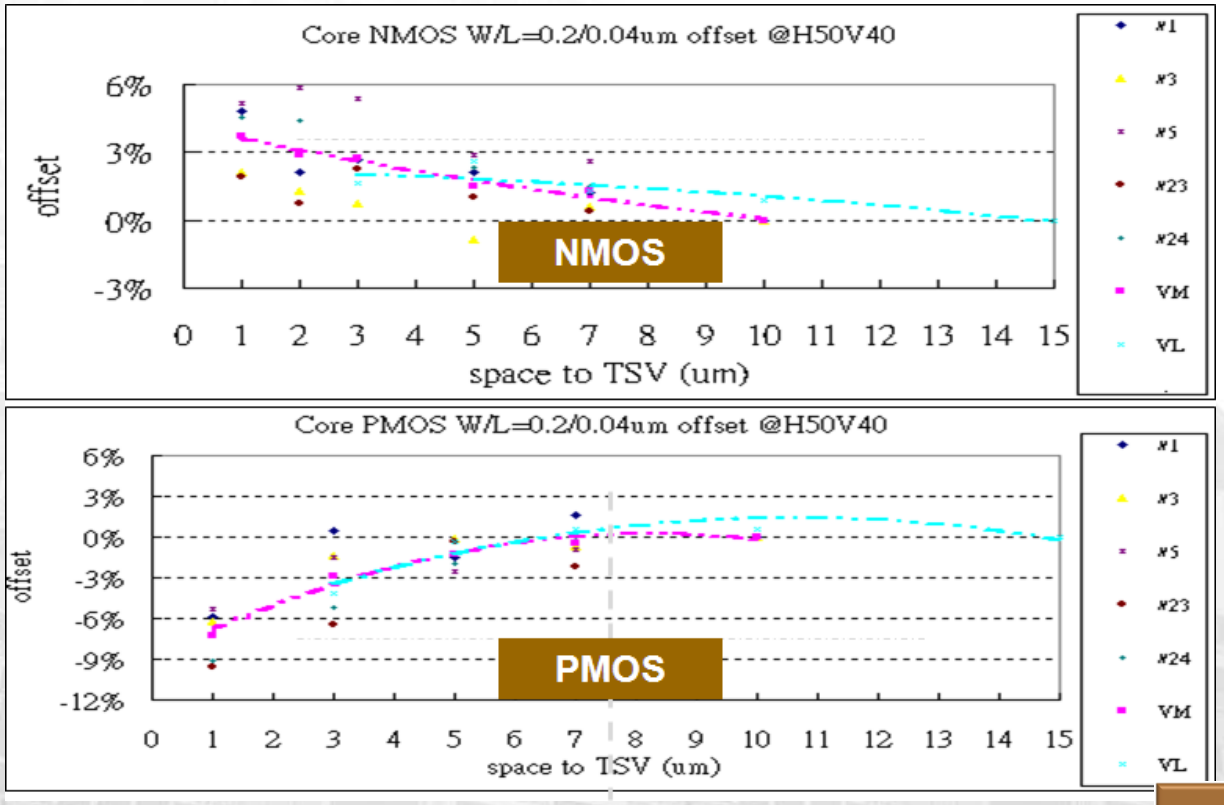




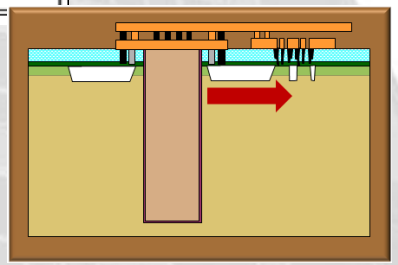
- Leakage effectively reduce

CMOS Impact Evaluation (3D)

- Keep-Out Zone (KOZ) Characterization

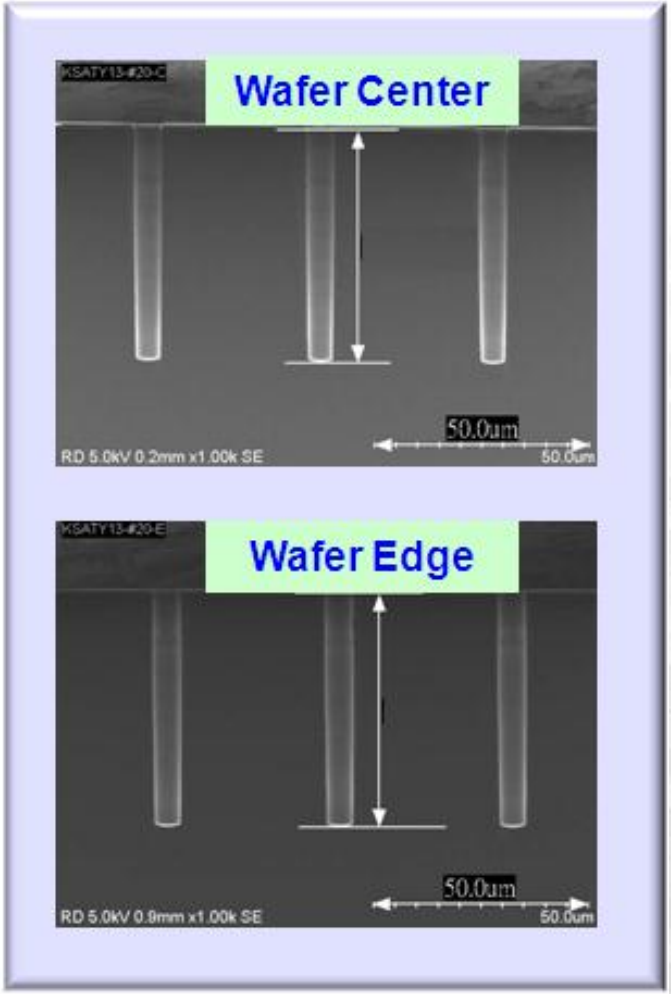


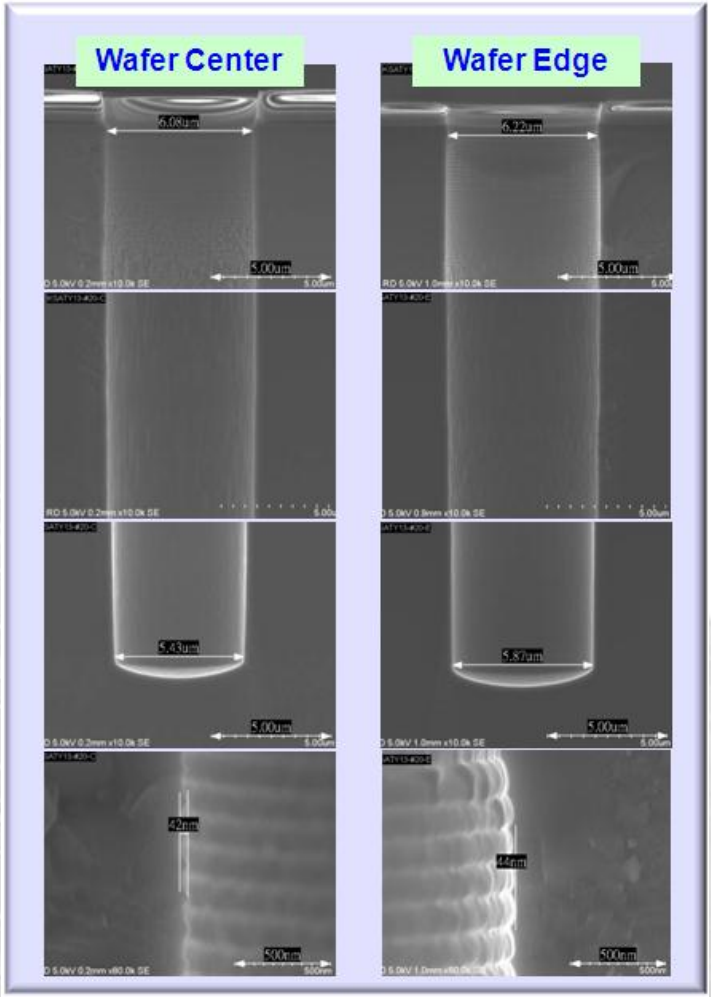
- KOZ: Dlon< 3% at distance >=5um
 - Device: 28nm HKMG core device
 - TSV pitch: JESD229 50/40um



Via Middle TSV (3D)

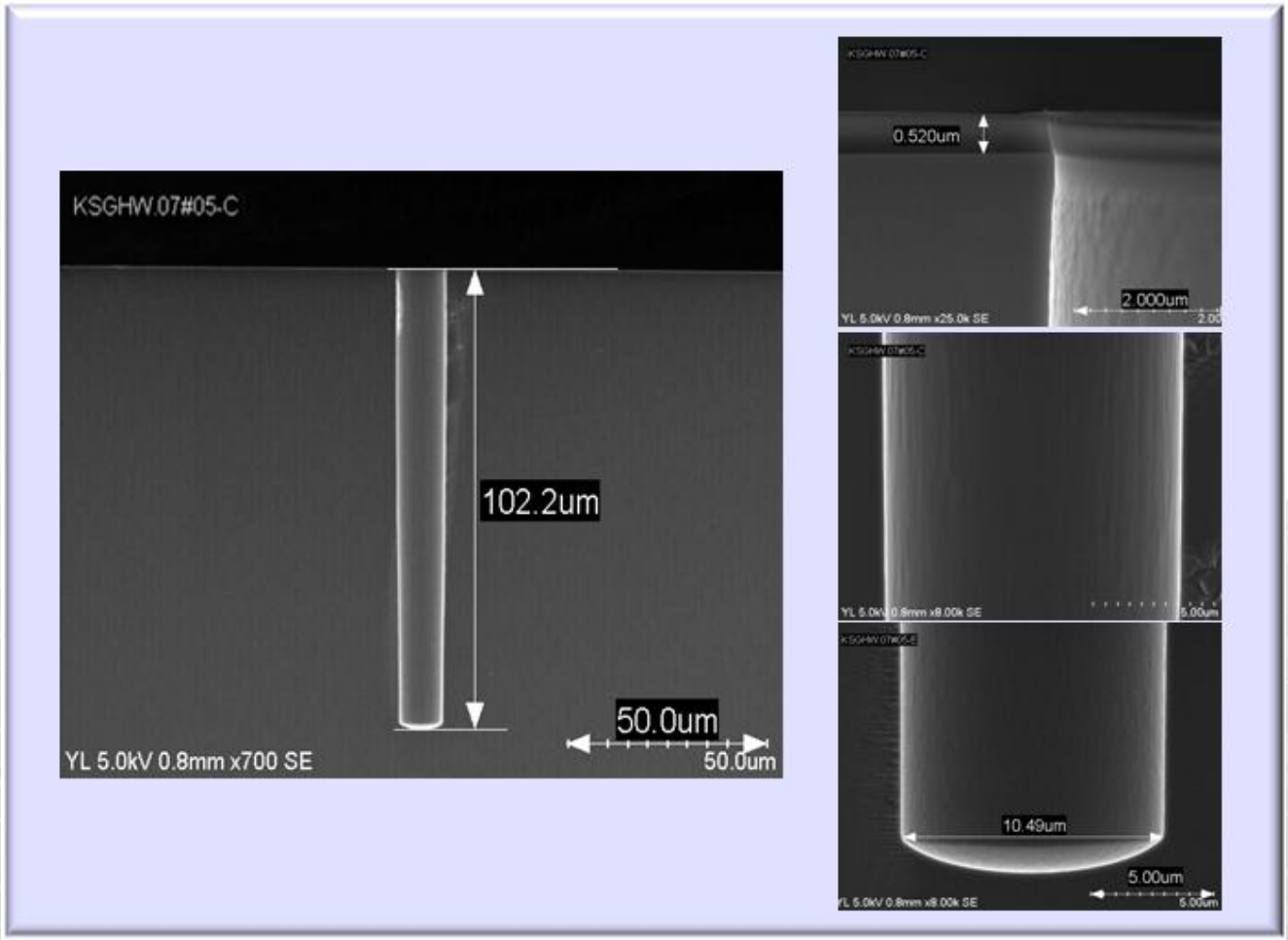
- 6um diameter, 54um depth





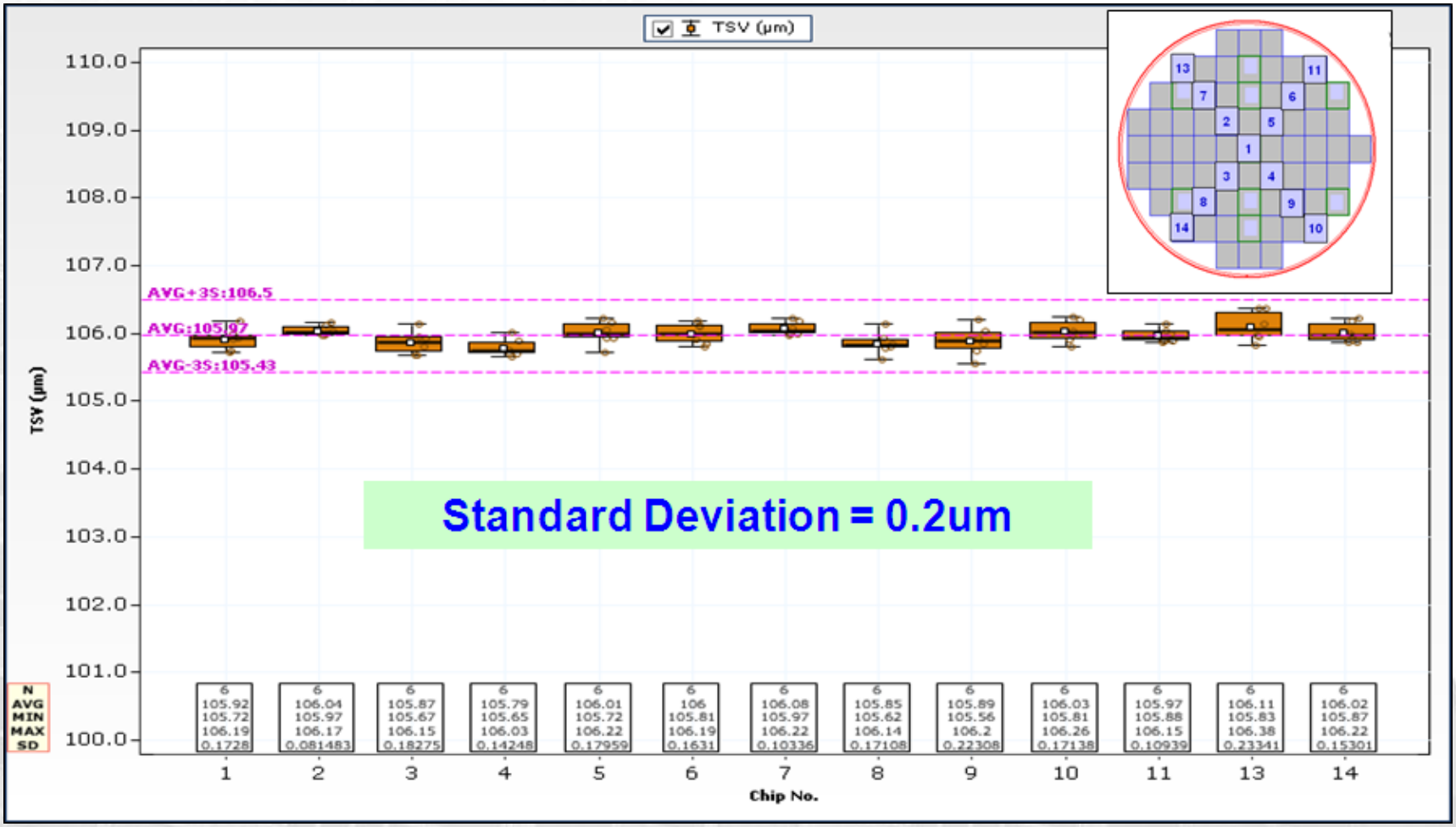
Si Interposer TSV (2.5D)

- 10um diameter, 100um depth



Uniformity Evaluation

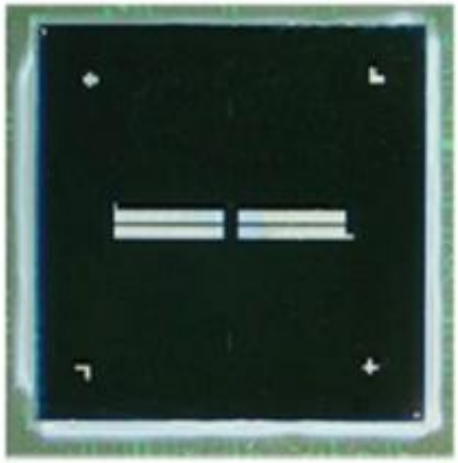
- 2.5D Si Interposer, 10x100um

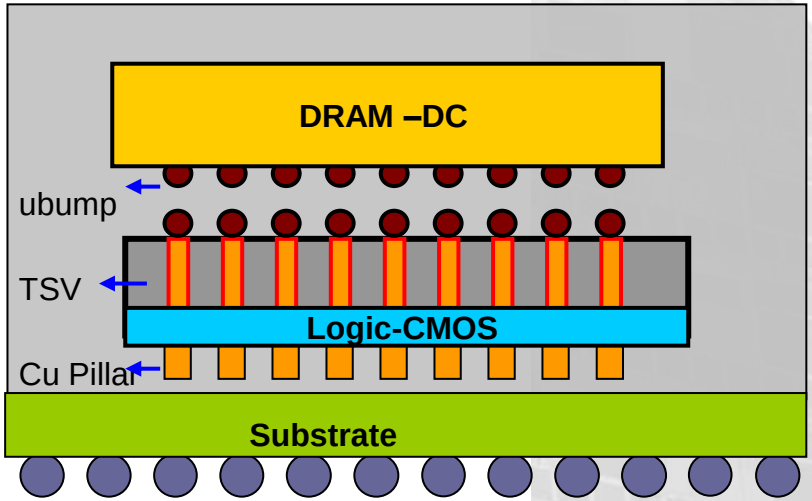


UMC 3D IC TV Stacking & Package



JEDEC WideIO interface



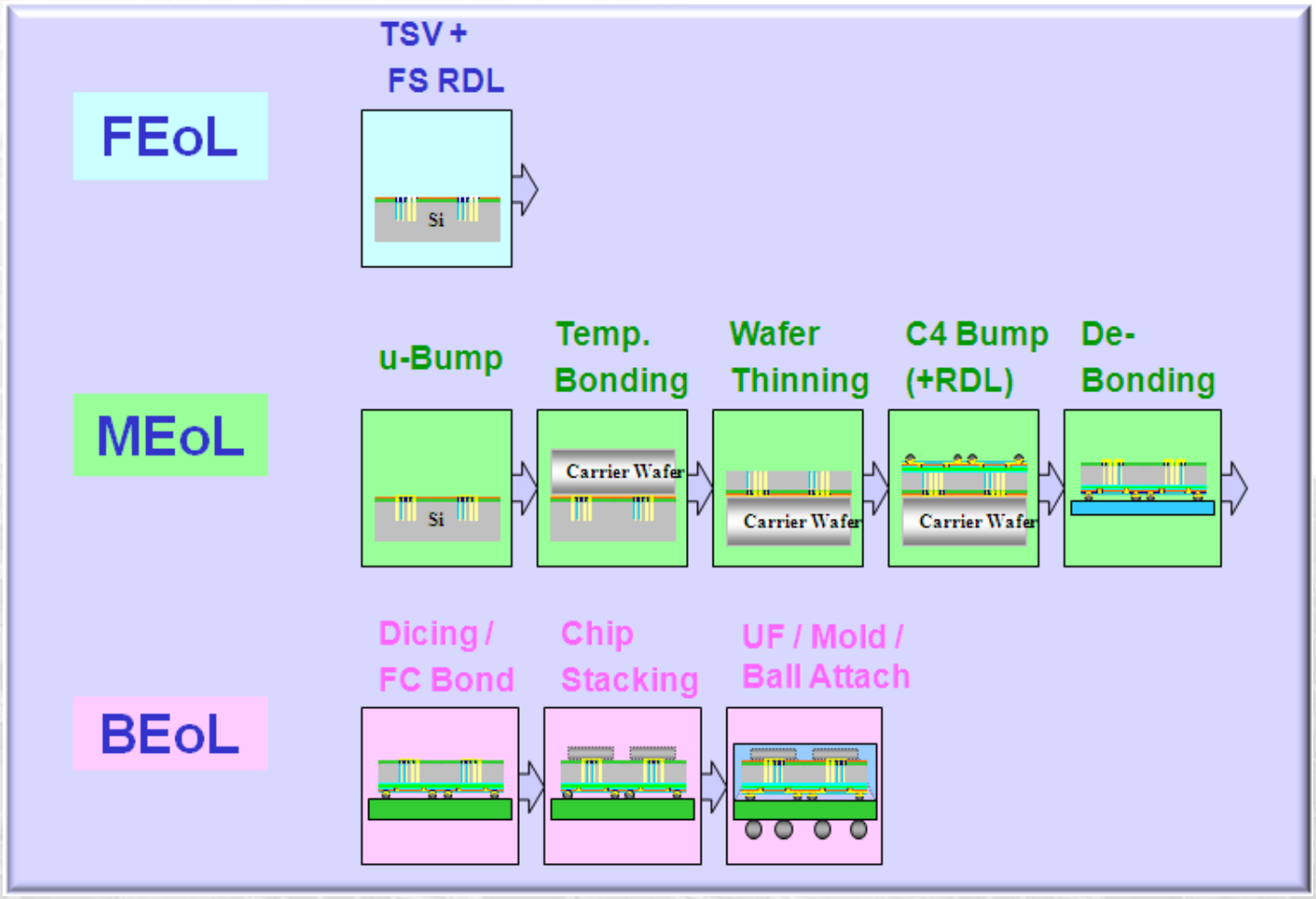


Ecosystem Work Flow

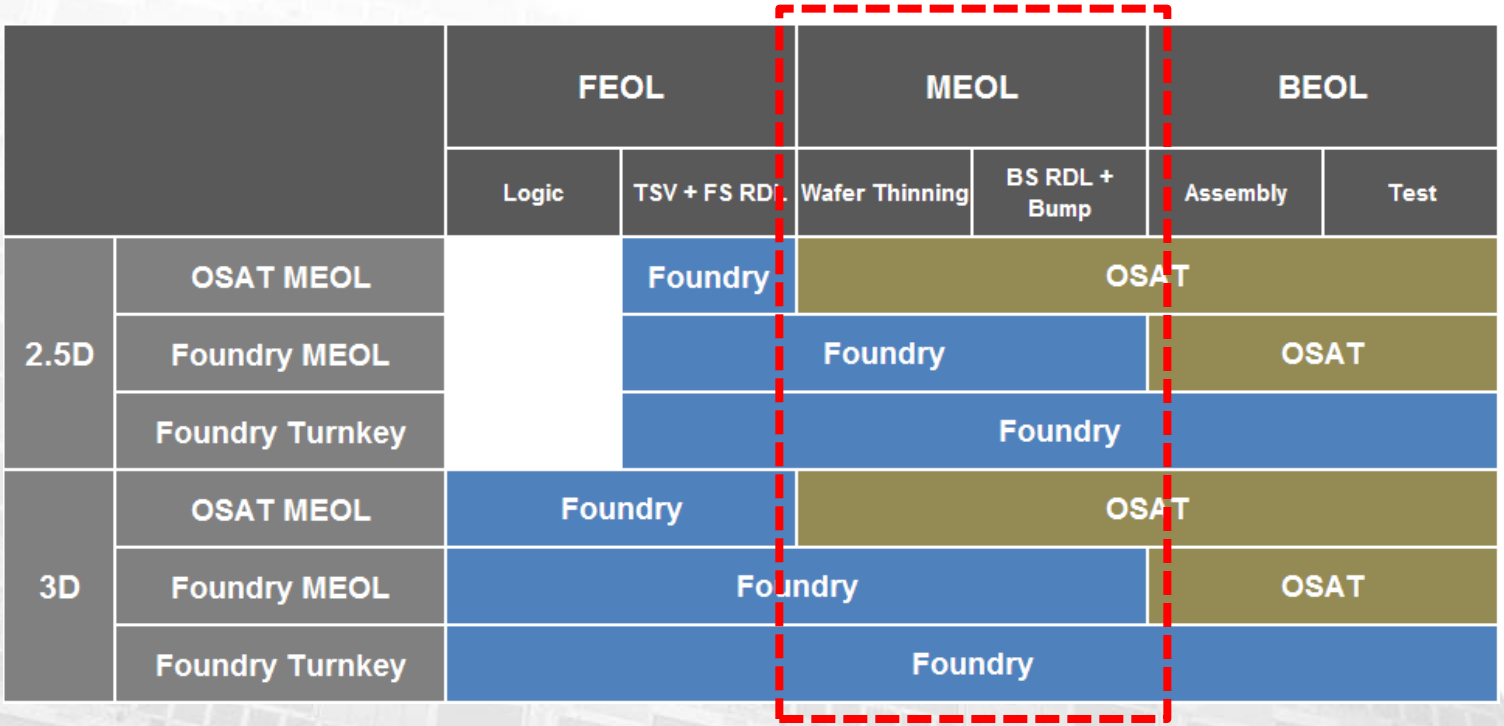
UMC

Customer-Driven Foundry Solutions

Example 2.5D Stacking Flow



Various Work Models



- Service scopes distinguished by MEOL inclusion
 - Consult your foundry/OSAT
- Work flow optimization may depend on BOM cost, stack recipe and test strategy

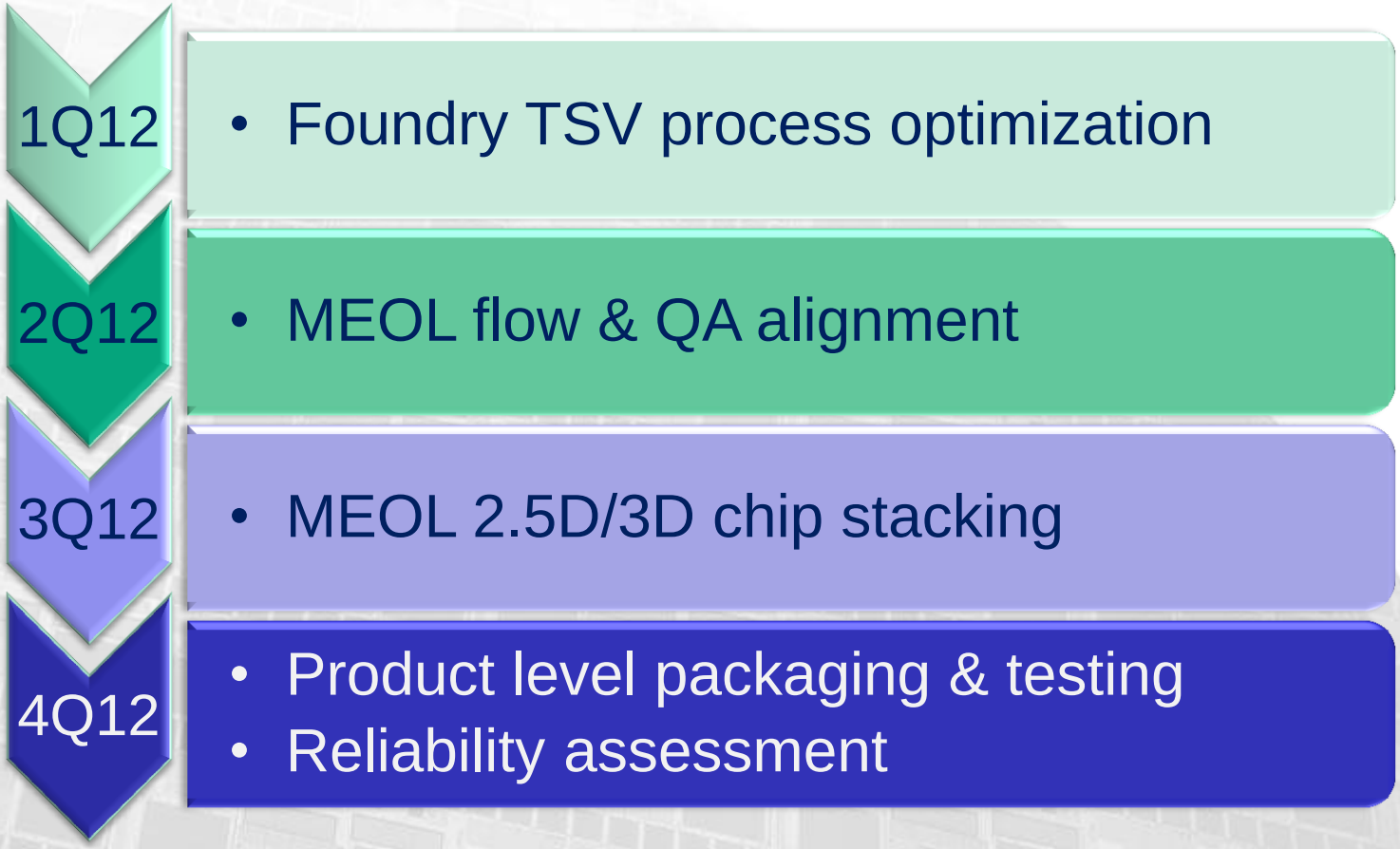
Foundry TSV Design Collaterals

Scheme	Feature Size				Document Status				
	TSV CD/Depth (um/um)	RDL Cu Layers	Cu Thickness /L /S (um/um/um)	Al Thickness (um)	Topologic Layout Rule	Electrical Design Rule	Interconnect Model	DRC Command File	LVS Command File
1.0um-wide	10/100	0.13 Inductor	2.0 /1.00/1.00	2.50	Ready	Ready	Ready	Ready	Ready
0.4um-wide	10/100	55nm 4X	0.8 /0.40/0.40	1.45	Ready	Ready	Ready	Ready	Ready
0.56um-wide	10/100	65nm 6X	1.25 /0.56/0.56	3.60	Ready	Ready	Ready	Ready	Ready

(UMC 2.5D Si interposer documents)

- Consider TSV a passive device with rule decks/models
 - Typical foundry engagement applies under ecosystem work flow

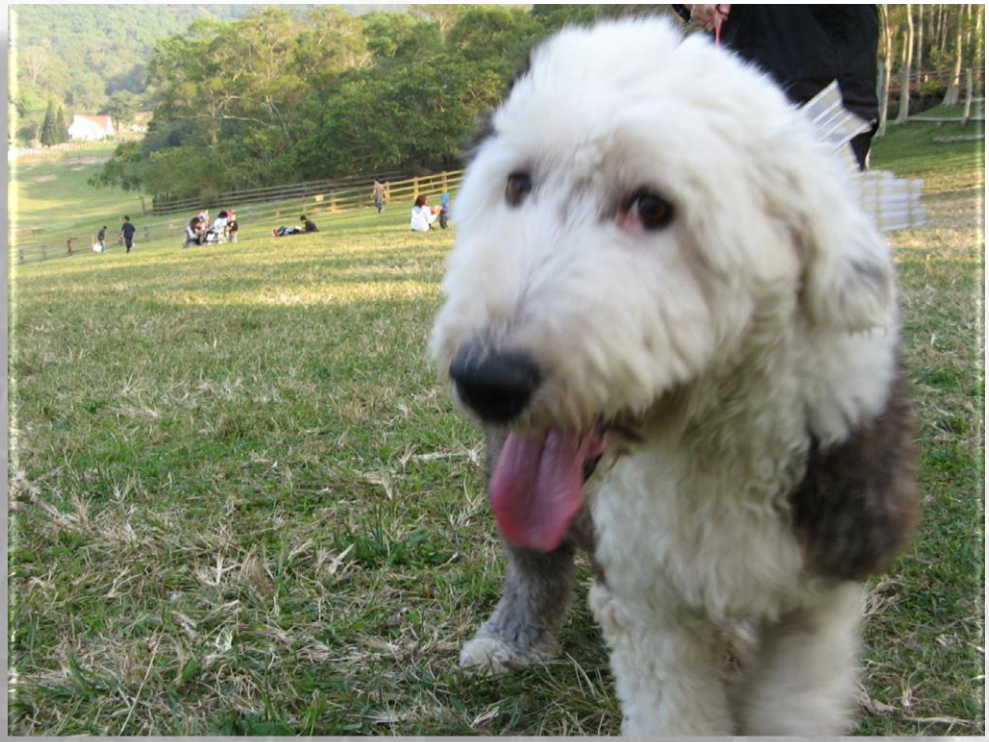
UMC Ecosystem Effort



Summary

Summary

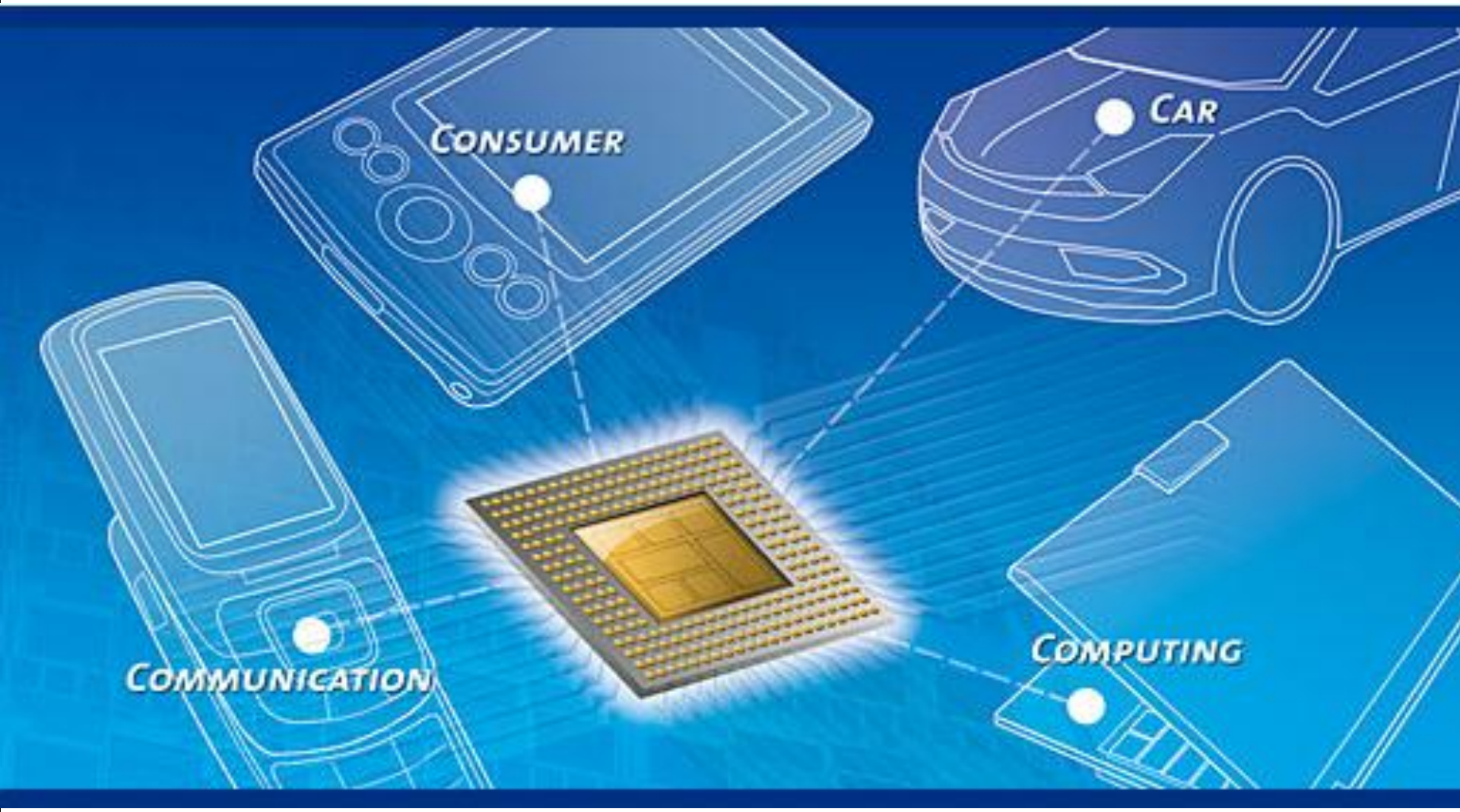
- Foundry TSV process demonstrated
 - Applicable to both 2.5D/3D
 - Leverage existing CMOS process technology
 - Key process issues identified & conquered
- Ecosystem work flow
 - Typical foundry/OSAT engagement flow applies for both 2.5D/3D, among other models
- Foundry TSV next step: ecosystem focus
 - Product level reliability assessment
 - Potential EDA collaboration for emerging 3D tools



Thank you for your attention!

Contact *foundry@umc.com* ***or*** *info@hotchips.org* ***.***

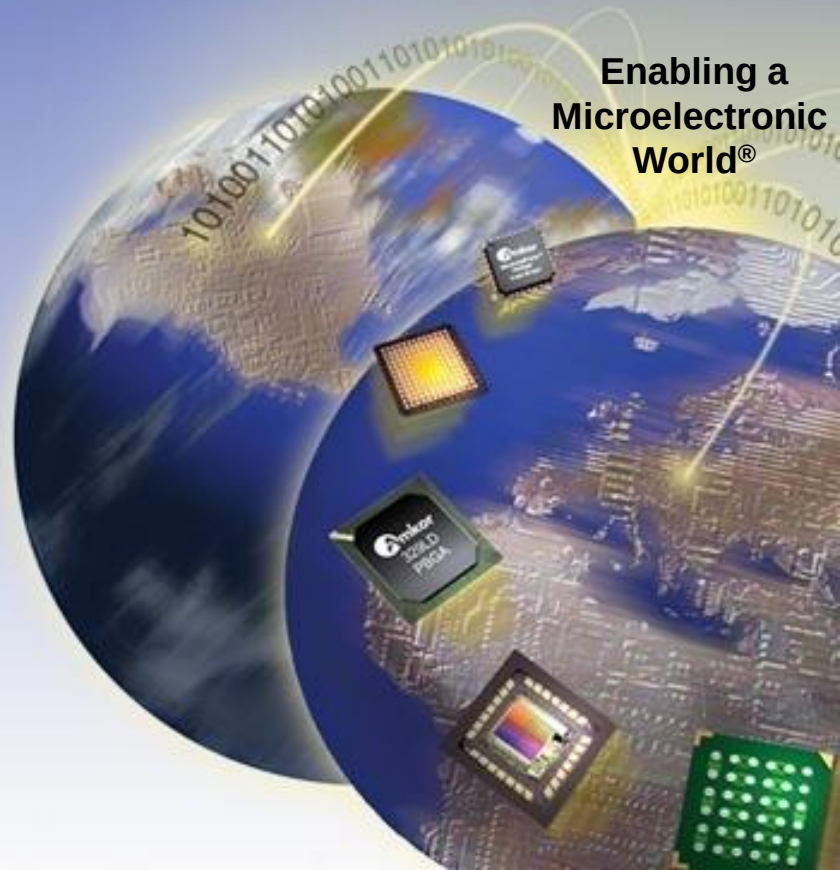
Thank You!



UMC

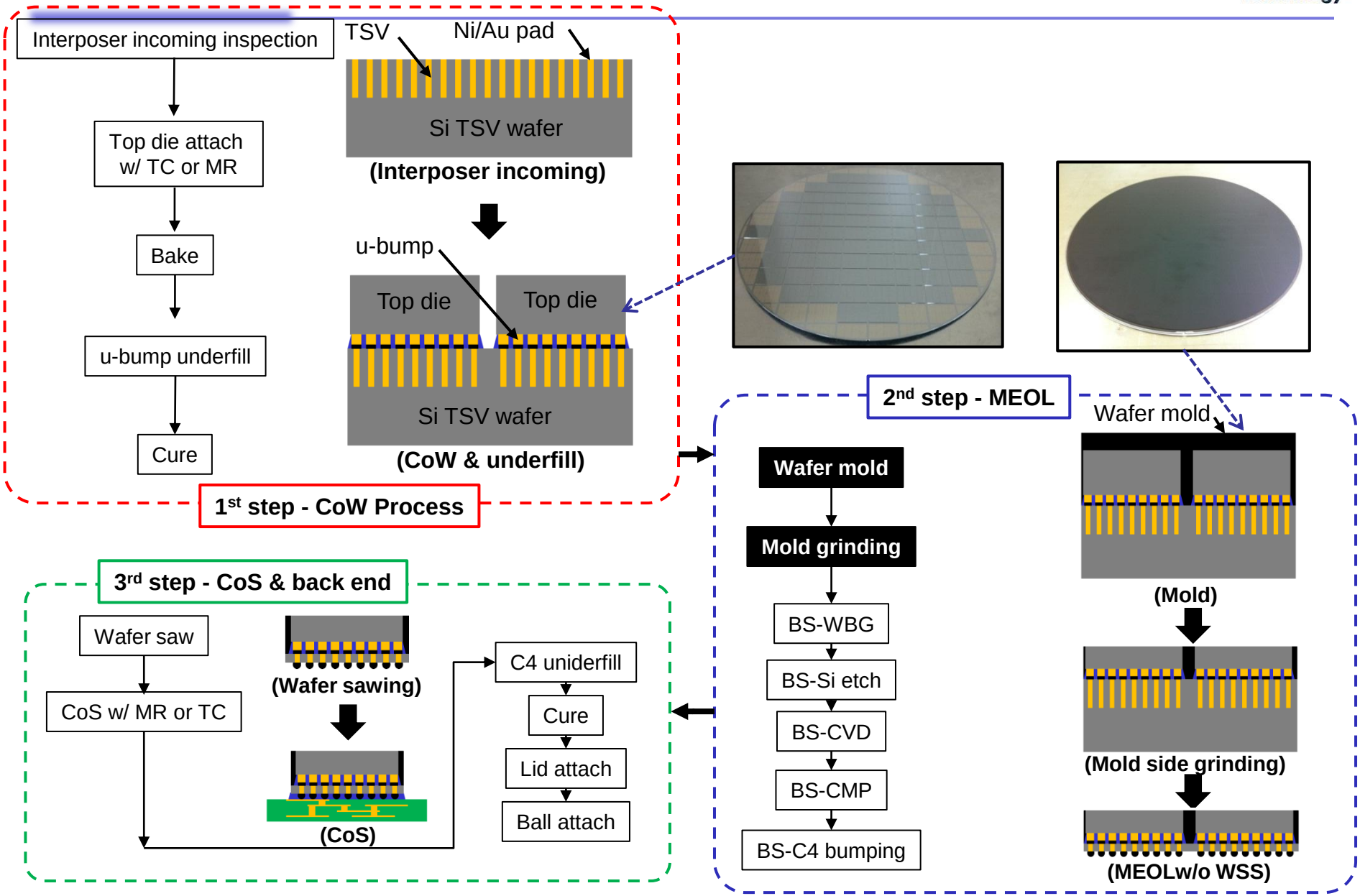
Full Processing Interposer Process

Hot Chips, Aug., 2012



Amkor Technology®

Chip on Interposer First Process



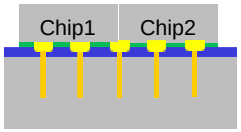
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Chip on Interposer First Process

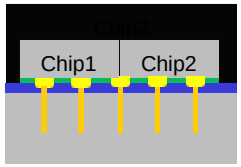
1 **Front Micro Bump Pad (Ni/Au)**



2 **Chip Attach & CUF**

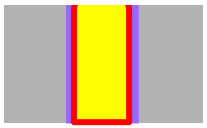


3 **Wafer Mold**



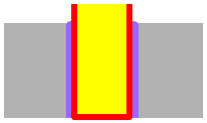
Organic Version

4 **Wafer thinning Flat reveal**



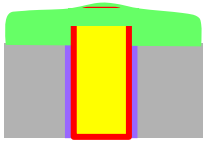
Cu reveal By WBG+CMP

5 **Silicon Recess**



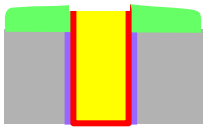
Dry etch : CF4

6-1 **Backside passivation**



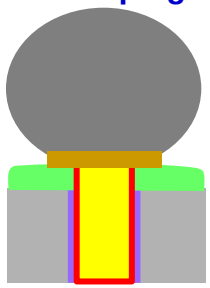
Pass. coat

7-1 **Secondary reveal**



Pass. exposure, Develop and cure

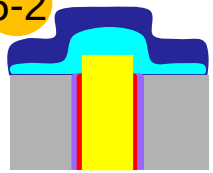
8 **C4 Bumping**



UBM +C4 plating

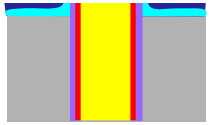
Inorganic Version

6-2

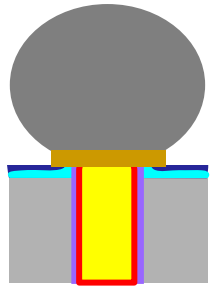


Inorganic passivation PECVD SiN + SiO2

7-2

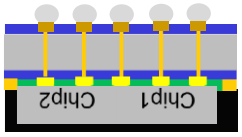


SiO2 CMP

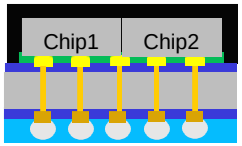


UBM +C4 plating

9 **Mold thinning**



10 **Dicing**



Chip Attach to Substrate

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Chip on Interposer First Process – High Level Risk

① **Front Micro Bump Pad**
 – Ni/Au Pad : Shape, Thickness, IMC embrittlement

② **Chip Attach & CUF : Chip Attach alignment, Flux cleaning, Underfill dispensing**

③ **Wafer Mold : Warpage, Void**

④ **Flat Reveal Wafer Thinning + CMP**
 – Wafer Cracking, Cu smearing, Cleaning

⑤ **Silicon Recess – Dry Etch (CF4)**
 – Cu corrosion, Etch rate variance, Slow Etch, Contaminate

⑥ **Passivation – organic pass. coating, PECVD**
 – Wafer Cracking, Edge Arcing, Thickness/Stress control

⑦ **Secondary Reveal –CMP : Wafer Cracking**

⑧ **C4 Bumping**

⑨ **Mold Thinning (optional)**

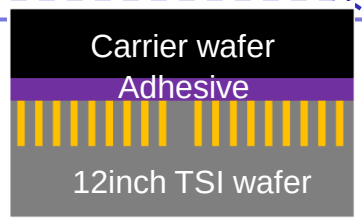
⑩ **Dicing – Saw street cracking**

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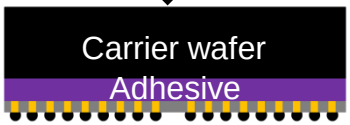
Chip on Interposer Last Process

1st step - MEOL

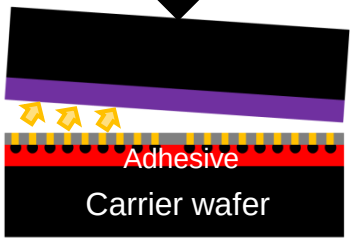
- Interposer incoming inspection
- WSS bonding
- BS-WBG
- BS-Si etch
- BS-CVD
- BS-CMP
- BS-C4 bumping
- WSS de-bonding and 2nd carrier bonding



(WSS bonding)



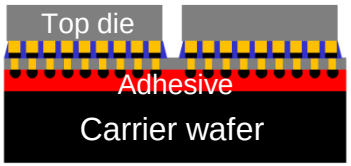
(MEOL & BS C4 bumping)



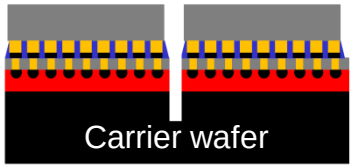
(WSS de-bonding & 2nd carrier bonding)

2nd step - CoW Process

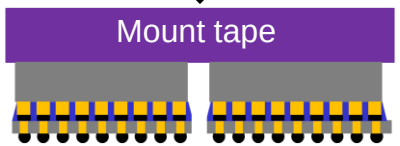
- Top die pick & place
- Mass reflow
- Underfill
- Cure
- Interposer saw w/ carrier
- De-bonding to mount tape



(Top die mass reflow & underfill)



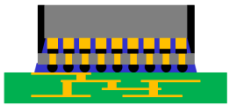
(Interposer saw)



(De-bonding to mount tape)

3rd step - CoS & back end

- CoS w/ MR or TC



(CoS)

- C4 uniderfill
- Cure
- Lid attach
- Ball attach

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Chip in interposer Last Process

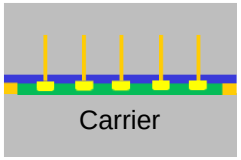
Organic Version

Inorganic Version

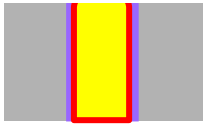
1 Front Micro Bump Pad (Ni/Au)



2 Zone bond

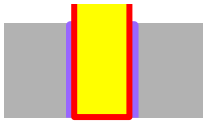


3 Wafer thinning Flat reveal



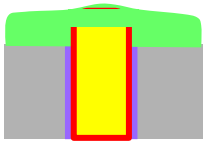
Cu reveal By WBG+CMP

4 Silicon Recess



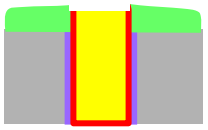
Dry etch : CF4

5-1 Backside passivation



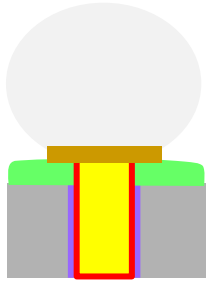
Pass. coat

6-1 Secondary reveal



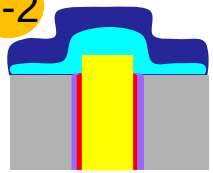
Pass. exposure, Develop and cure

7 C4 Bumping



UBM +C4 plating

5-2

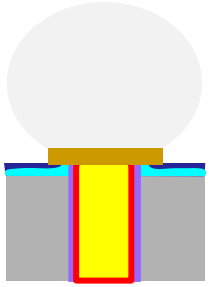


Inorganic passivation PECVD SiN + SiO2

6-2

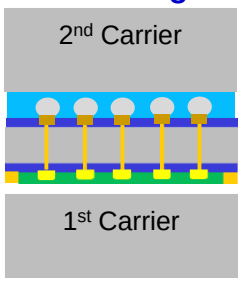


SiO2 CMP

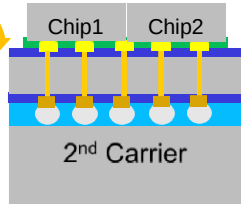


UBM +C4 plating

8 2nd Carrier Bonding & 1st Carrier De-bonding



9 Chip Attach &CUF



2nd Carrier De-bonding, Dicing

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Chip on Interposer Last Process – High Level Risk

① **Front Micro Bump Pad**
- Ni/Au Pad : Shape, Thickness, IMC embrittlement

② **Zone Bond : TTV Control**

③ **Flat Reveal Wafer Thinning + CMP**
- Wafer Cracking, Cu smearing, Cleaning

④ **Silicon Recess – Dry Etch (CF4)**
- Cu corrosion, Etch rate variance, Slow Etch, Contaminate

⑤ **Passivation – Organic pass. coating, PECVD**
- Wafer Cracking, Edge Arcing, Thickness/Stress control

⑥ **Secondary Reveal**
- Wafer Cracking

⑦ **C4 Bumping**

⑧ **2nd Carrier Bonding & 1st Carrier De-bondding**

⑨ **Chip Attach on Interposer**

⑩ **2nd Carrier de-bonding**

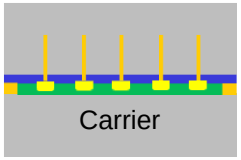
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TSV - Interposer M/BEOL Process

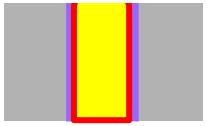
1 Front Micro Bump Pad (Ni/Au)



2 Zone bond

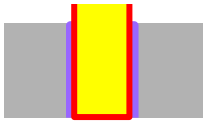


3 Wafer thinning Flat reveal



Cu reveal By WBG+CMP

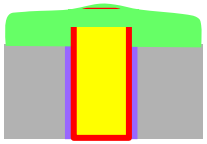
4 Silicon Recess



Dry etch : CF4

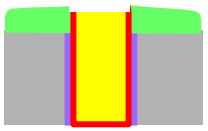
Organic Version

5-1 Backside passivation



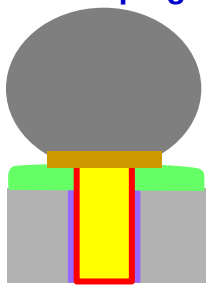
Pass. coat

6-1 Secondary reveal



Pass. exposure, Develop and cure

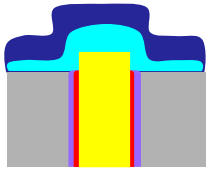
7 C4 Bumping



UBM +C4 plating

Inorganic Version

5-2

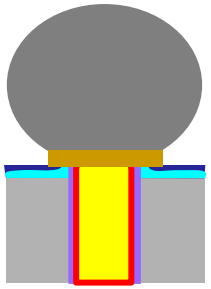


Inorganic passivation PECVD SiN + SiO2

6-2

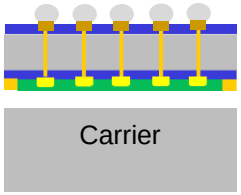


SiO2 CMP



UBM +C4 plating

8 Zone Bond De-bonding



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Interposer Process – High Level Risk

① **Front Micro Bump Pad**
- Ni/Au Pad : Thickness, IMC embrittlement

② **Zone Bond**
- TTV Control

③ **Flat Reveal Wafer Thinning + CMP**
- Wafer Cracking, Cu smearing

④ **Silicon Recess – Dry Etch (CF4)**
- Cu corrosion, Etch rate variance, Slow Etch, Contaminate

⑤ **Passivation – Organic pass. coating, PECVD**
- Wafer Cracking, Edge Arcing, Thickness/Stress control

⑥ **Secondary Reveal**
- Wafer Cracking

⑦ **C4 Bumping**

⑧ **Carrier De-bondding**
- Wafer Breakage

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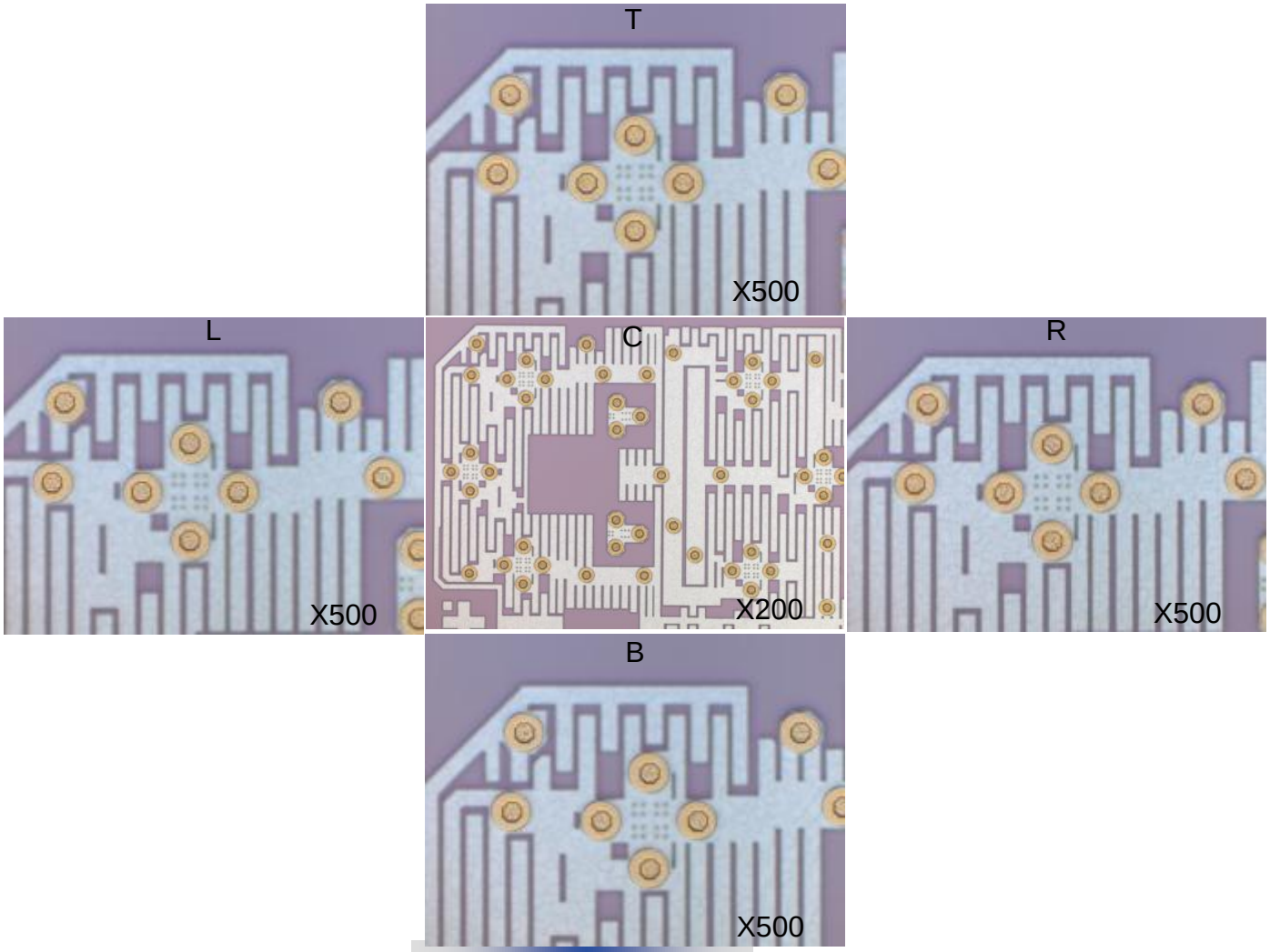
1. FS NiAu – CoC Evaluation

- **CoC Evaluation on E-lytic Ni/Au**
 - AOI inspection
 - Ni/Au thickness measurements
 - Auger analysis for surface condition
 - Wafer bonding
 - Simulated backside thermal processes
 - Debond
 - AOI Pad inspection for FM
 - Singulate
 - Mass Reflow
 - TC Bond
 - "FA - X-section, EDX line scan, EDX area mapping"
 - TC CoC
 - FA

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FS NiAu Plating Evaluation

- **Images - Post UBM Etch Process**
 - There are no abnormalities



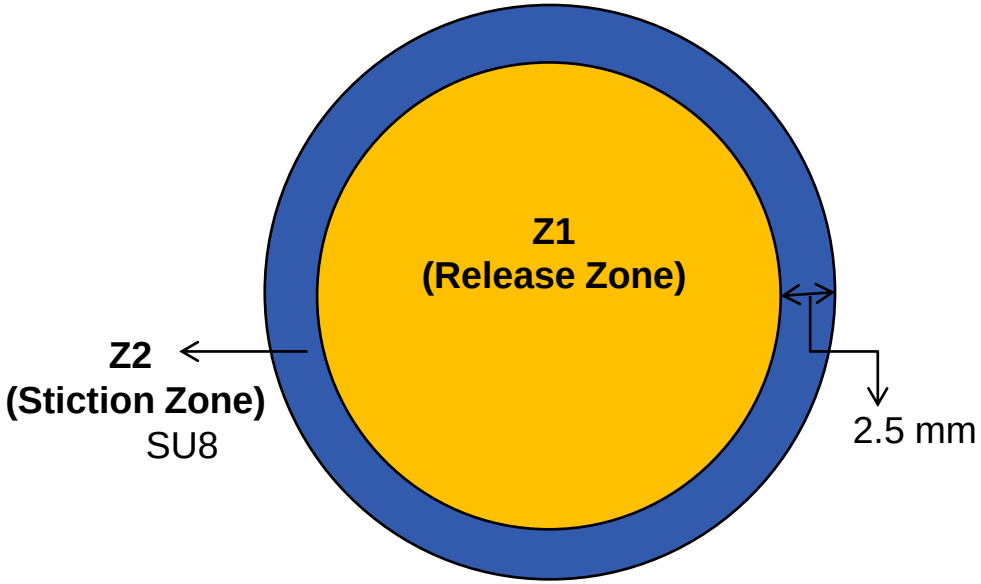
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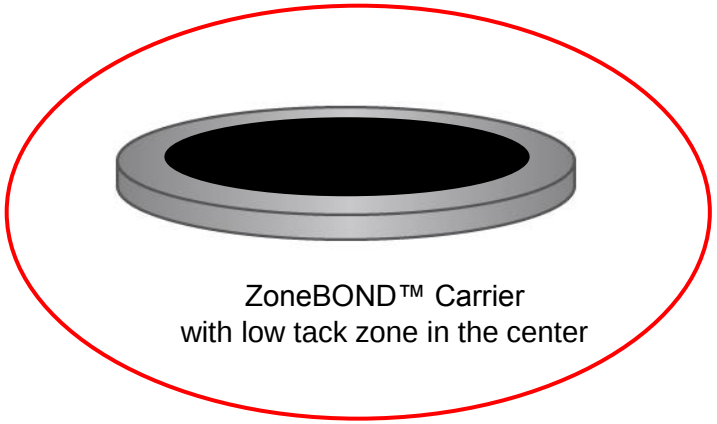
Edge trim & WSS

- **Process validation**
 - For edge trimming to reduce chipping.
 - Optimization of wafer bonding to minimize thickness variance of temporary bonding adhesive.
 - Minimizing wafer crack on debonding process.
 - EAR optimization

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Overview of ZoneBOND carrier wafer





- **Silane+FC40 (Z1, release zone)**
 - This is anti-sticky zone.
- **Edge zone (Z2, stiction zone)**
 - Edge zone width is approximately 2.5mm.
 - Minimum edge zone width is 1.5 mm.
 - SU8 is used as the edge zone mask.

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Zone treated Carrier Preparation

- **Drop test to Acetone**



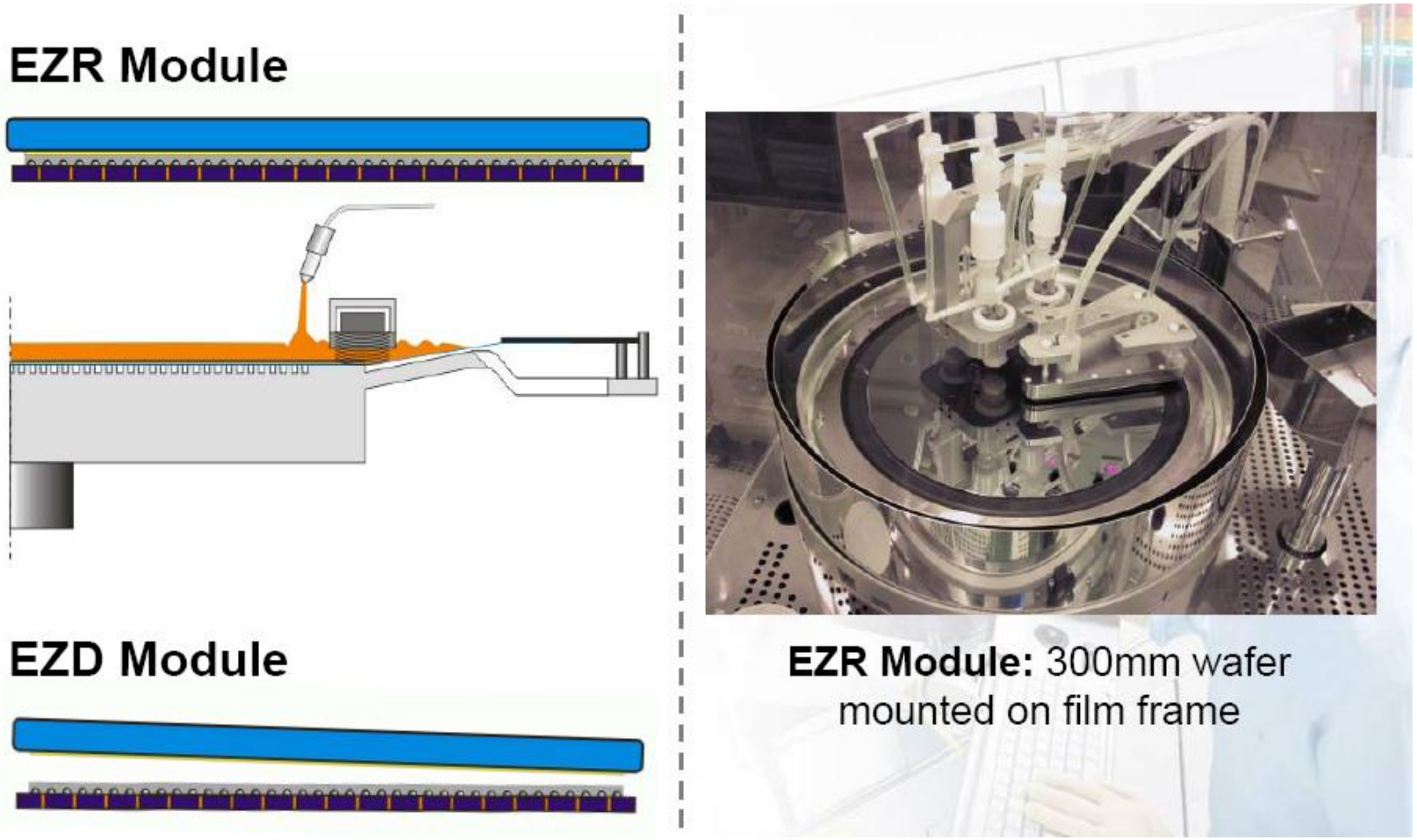


 - We can confirm that Zone treated carrier wafer(Z1) to acetone.
 - Z1 is non stick. The reaction of the material to the wafer is just to make the material chemically bond to the wafer that as a “Silanol condensation reaction”. Once it reacts with the surface, the single molecule layer that’s permanently attached to the carrier acts as a poly tetrafluoroethylene(PTFE) or “ Teflon like” coating on the wafer.

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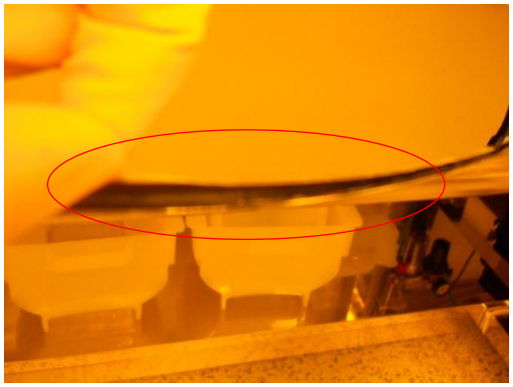
ZoneBOND De-bonding

- **Edge Zone Release with EZR & EZD module**



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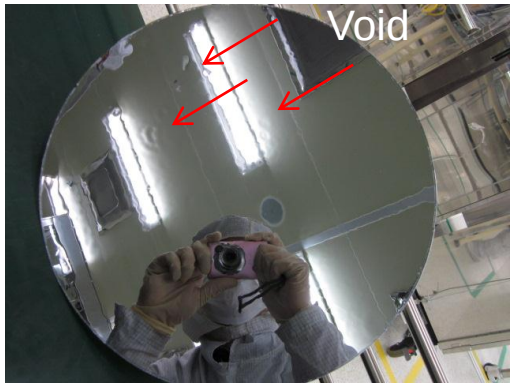
Failures & Problems Related with ZoneBOND De-Bonding



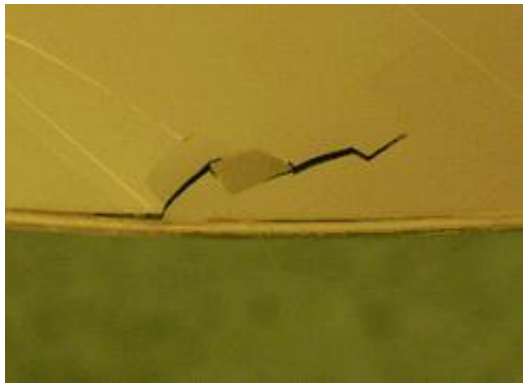
→Delamination



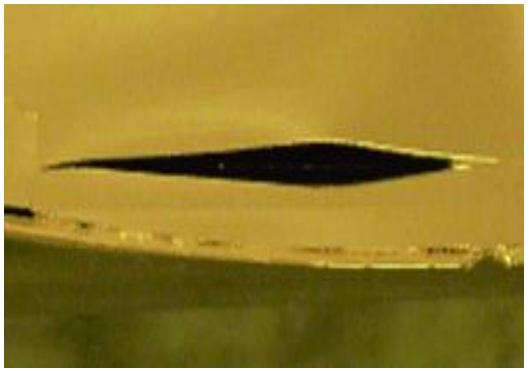
→Adhesive squeeze out



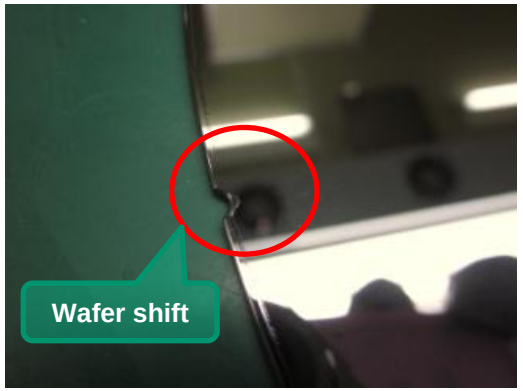
→Blisters



→Crack at edge zone



→Crack



→Wafer shift

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World Wide Temporary Bonding Methods

	Thermal	Zone	Laser	Chemical	Wedge
Machine	EVG, TEL, SUSS	EVG, SUSS	TAZMO, Yushin, SUSS	TOK	SUSS
Material	BSI, ShinEtsu, Sumitomo	BSI, ShinEtsu, Sumitomo	3M	TOK	TMAT, Dow
Machine price	Middle	High	Middle	Middle	High
Material price	High	High	Middle	High	Middle
TTV	Good	Normal	Good	Normal	Normal
UPH	Middle	Low	High	Low	High

DUPONT The miracles of science™
HD-3007



SUSS XBC300

brewer science
ZoneBOND™

ThinMaterials
Material made by WACKER

3M
Wafer Support System

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Advantage & Disadvantage of Various Methods

POR NEW

System		Thermal	Zone	Laser	Chemical	Wedge
Bond	Advantage	- Using the Si carrier	- Using the Si carrier	- Using the UV cure - Low out gassing - Double side bond	- 1 layer adhesive coat - Short bonding time - Good to adhesive generality	- Using the Si carrier - Development of an active adhesive
	Dis advantage	- Long Bonding time	- Application of Zone carrier - Bad to adhesive stability - High machine price	- Using the Glass carrier - Bad to adhesive generality	- Using the hole Glass carrier - Coating the top device - High carrier price	- 2 layer coat - Difficult to control adhesion - High machine price
Bump process	Advantage	- Applicable issue to the Si carrier	- Applicable issue to the Si carrier	- High stability (thermal, chemical)	- Advantage of out gassing - High chemical stability	- Applicable issue to the Si carrier
	Dis advantage	- Bad thermal stability - High adhesive contamination	- Bad thermal stability - Change the adhesive - Weak to void	- Glass chucking - Weak to void	- Glass chucking - Bad thermal stability - Process failure by high warp	- Low adhesion - Concern to Si del. - Weak to void - High adhesion contamination
Debond	Advantage	- No mount tape damage	- Room temperature debond - High thermal stability	- Room temperature debond	- High thermal stability	- Room temperature debond -Carrier remove to short time -High thermal stability
	Dis advantage	- Need to high temperature process - Bump damage - Thin wafer handling	- Long remove time to edge adhesion - Worry about new process - High machine price	- Possibility to laser damage - Difficult to rework - Adhesion change at surface	- Long time of adhesion removal - After removing the adhesion, possibility of damage	- Wafer edge damage - High machine price

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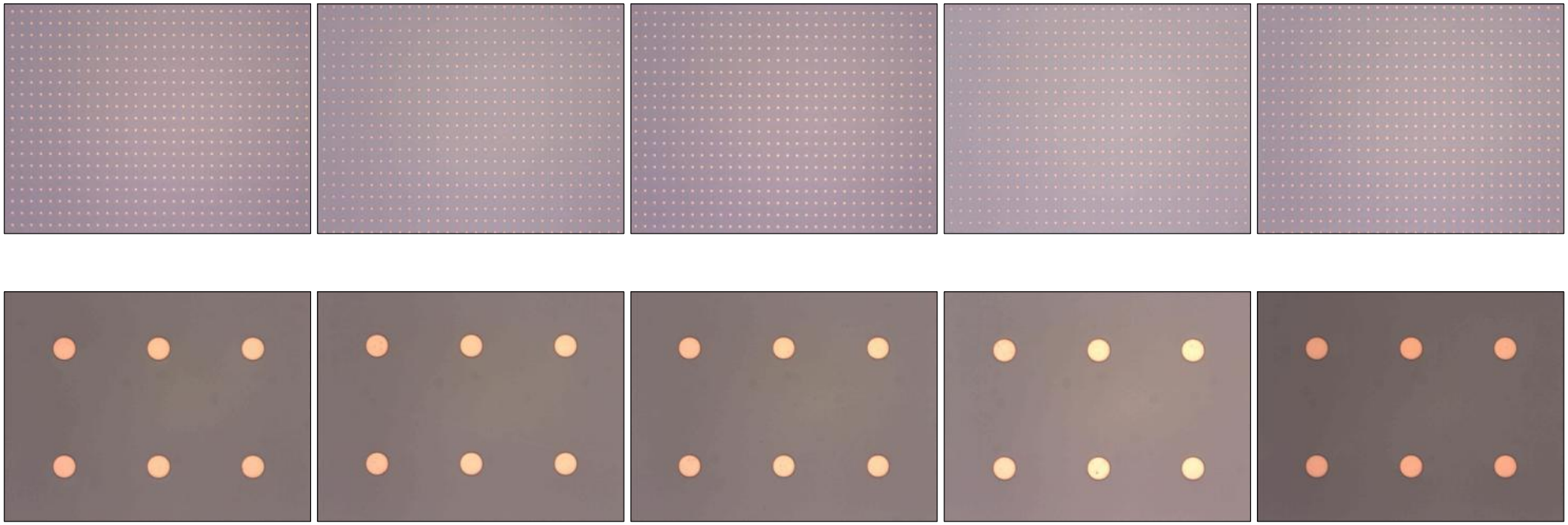
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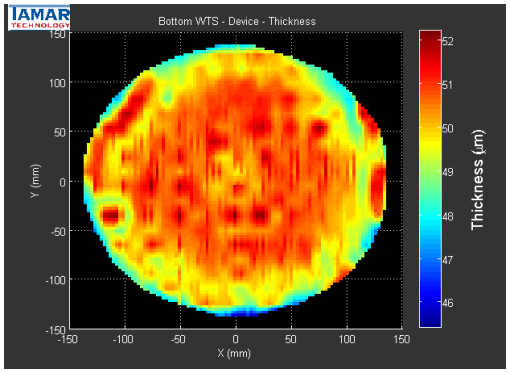
WBG and Cleaning

- **Process validation**
 - Soft reveal
 - Minimizing TTV with accurate control.
 - Cleaning improvement after wet polish.
 - Flat process
 - Only grinding of Si layer at WBG tool not to expose Cu.
 - Using CMP tool to expose Cu and post CMP cleaning

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Wafer Thinning & Cleaning
Example of Flat process





<Device>

Mean : 50.1 um
Max : 52.7 um
Min : 46.8 um
TTV : 5.9 um

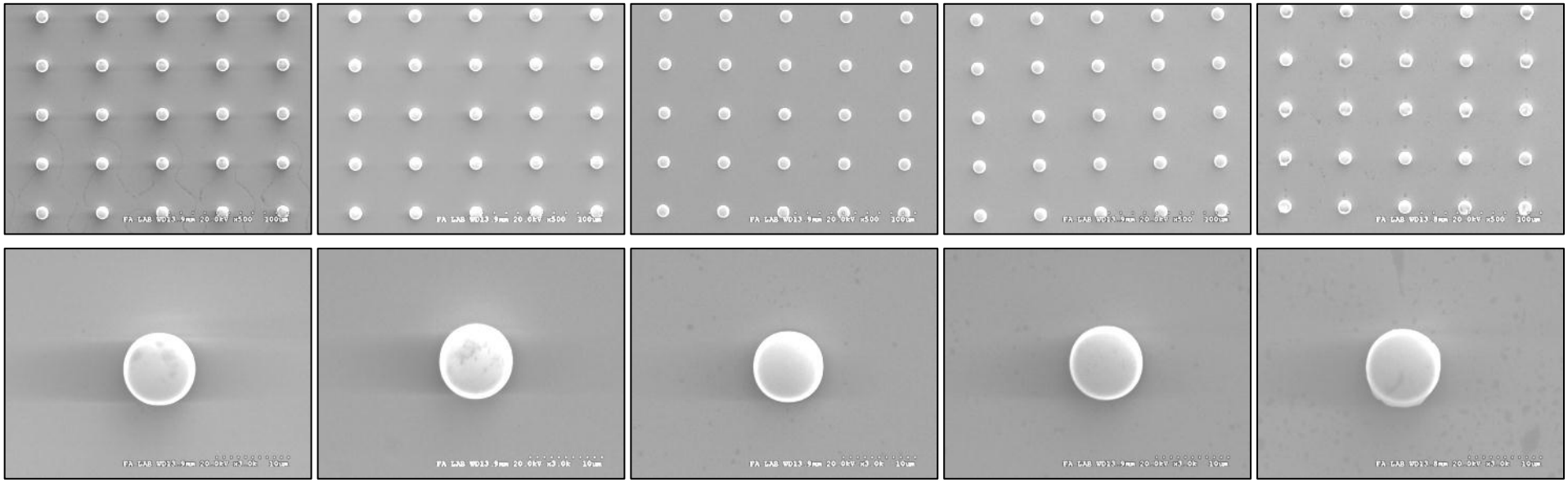
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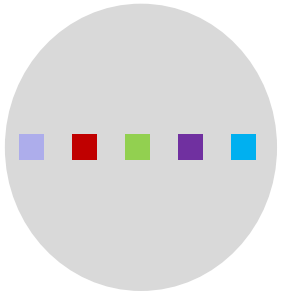
Dry Etch

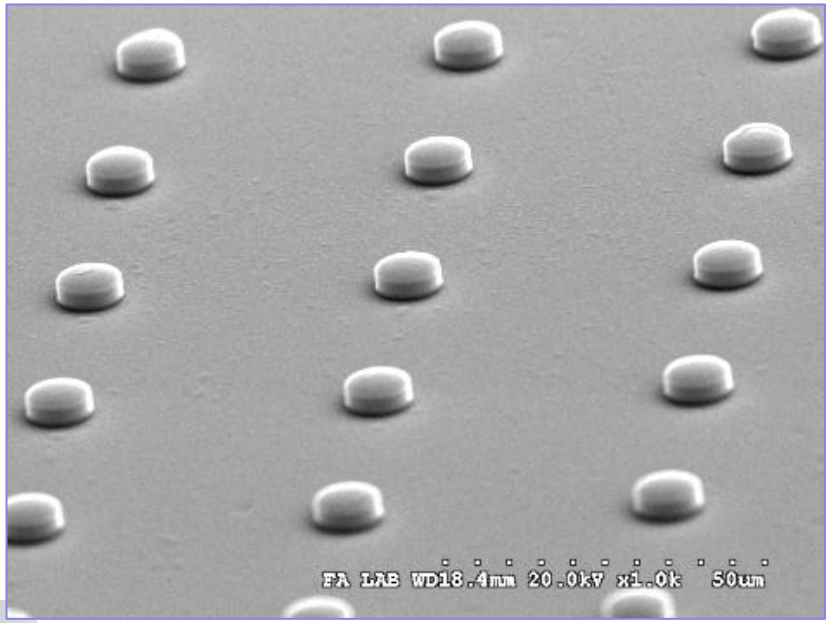
- **Process validation**
 - Soft reveal
 - Acceptable etch rate
 - Optimizing etch rate and uniformity with TSV bonded pairs.
 - Finding via height for ISR process sequence.
 - Flat process
 - Very slow etch rate
 - Optimizing etch rate and uniformity with TSV bonded pairs
 - Etch gas mixing evaluation to improve etch rate without Cu corrosion.

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Si recess etching : Dry etch





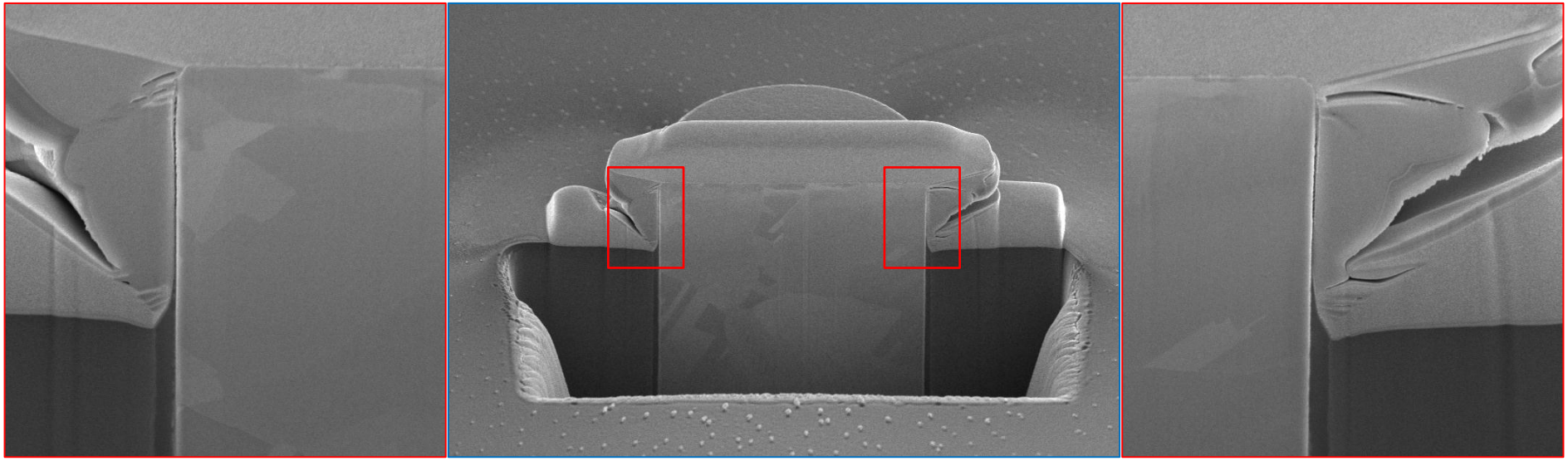


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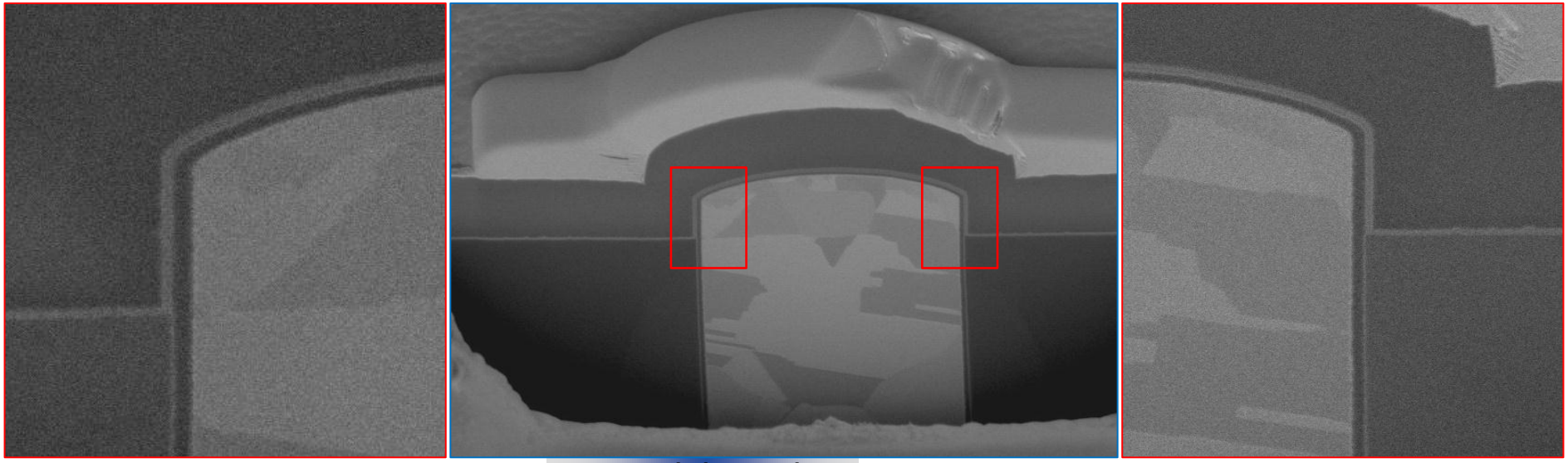
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Si recess etching : Dry etch

➢ Flat process



➢ Soft reveal process



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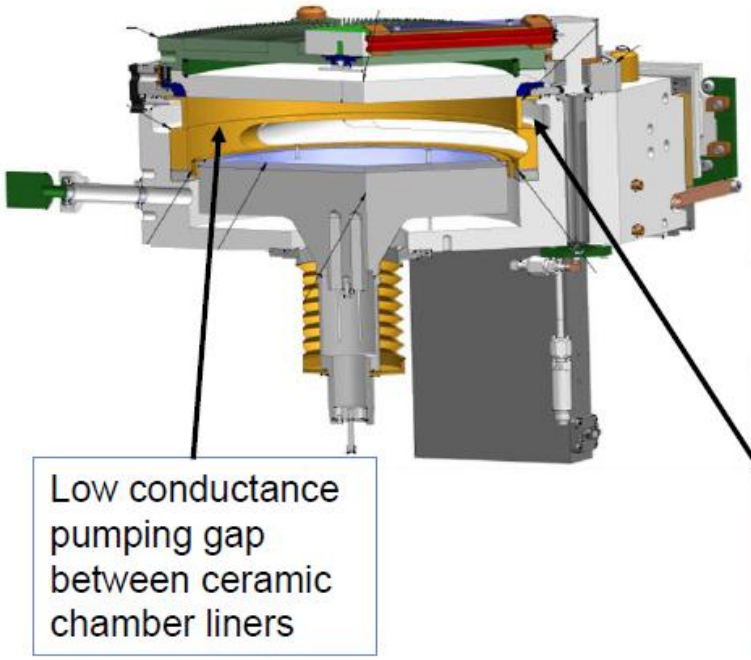
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PECVD

- **Process validation**
 - Deposition of SiN and SiO2
 - Confirming deposition rate, uniformity, stress and RI.
 - Setting up measurement method using elipsometer to check single layer, multi layer.

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Dielectric deposition : PECVD

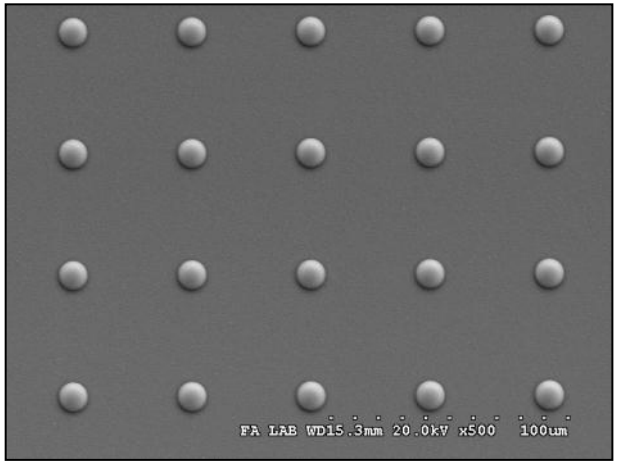


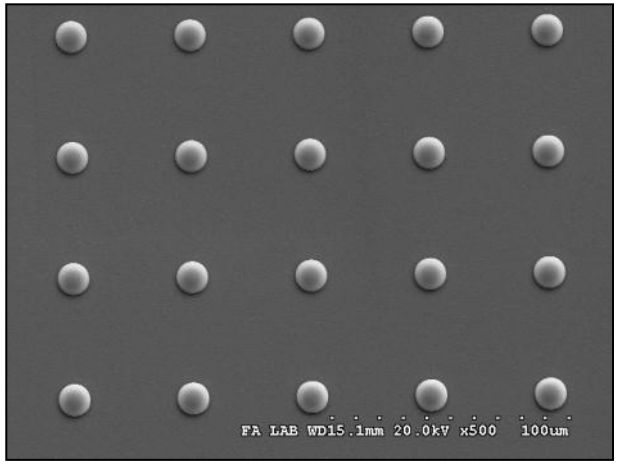
- Pumping gap limits conductance
- Extends 360°
- Radially symmetrical pumping
- Large volume pumping gallery
- Uniformity unaffected by pump

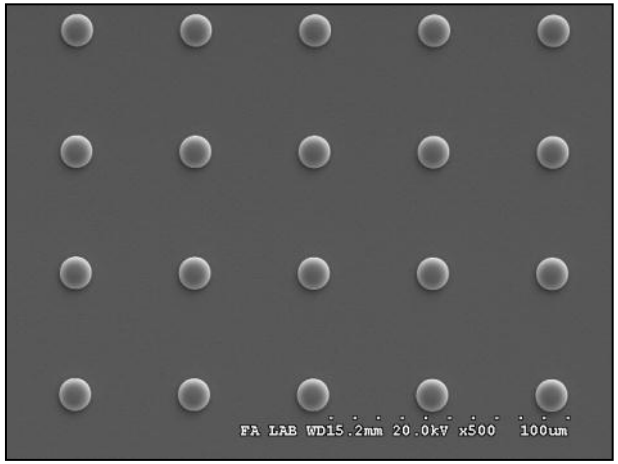
- Silicon Nitride
 - $SiH_4(g) + NH_3(g) + N_2(g) \rightarrow Si_xN_yH_z(s) + H_2(g)$
- Silicon Oxide [Silane-based process]
 - $SiH_4(g) + 4N_2O(g) + N_2(g) \rightarrow SiO_2(s) + 4N_2(g) + H_2(g) + O_2(g)$
- Silicon Oxide [TEOS-based process]
 - $Si(OC_2H_5)_4(g) + O_2(g) \rightarrow SiO_2(s) + \text{byproducts}$

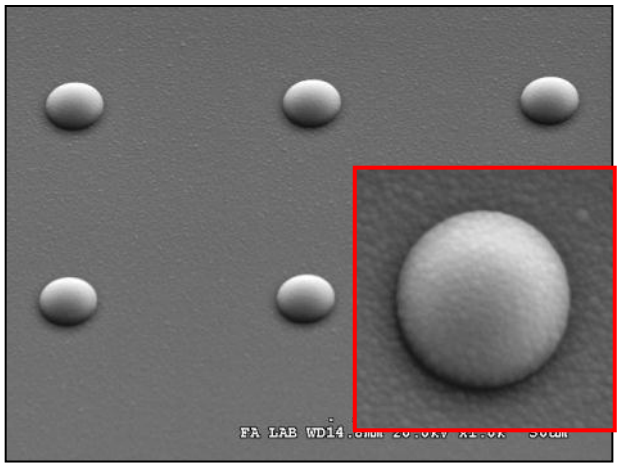
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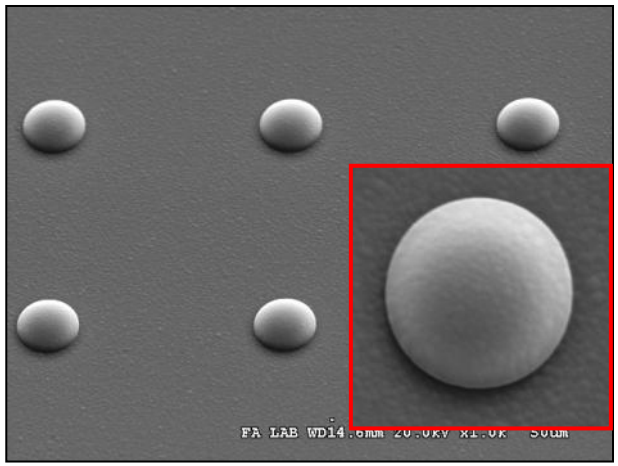
Dielectric deposition : PECVD

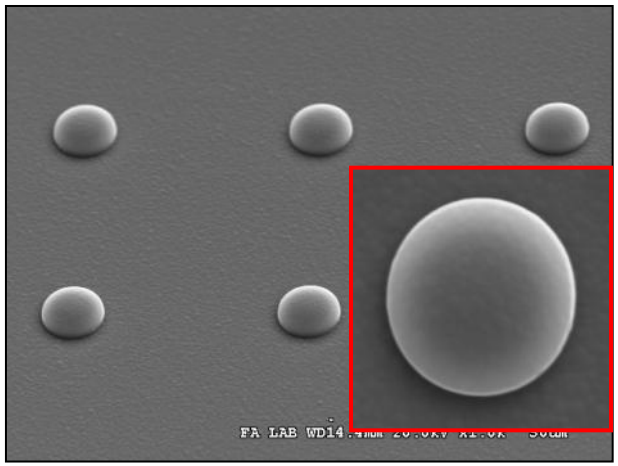












Center

Middle

Edge

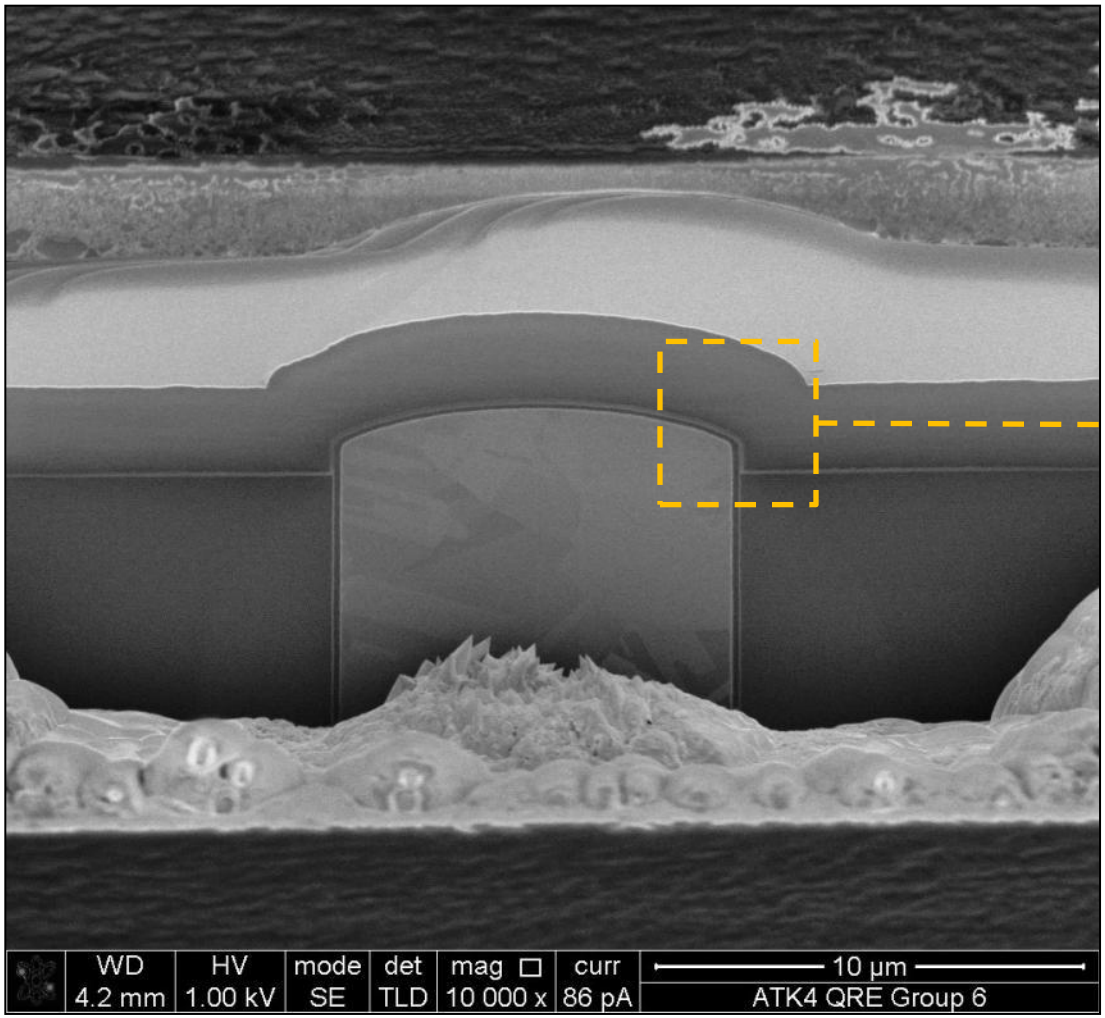
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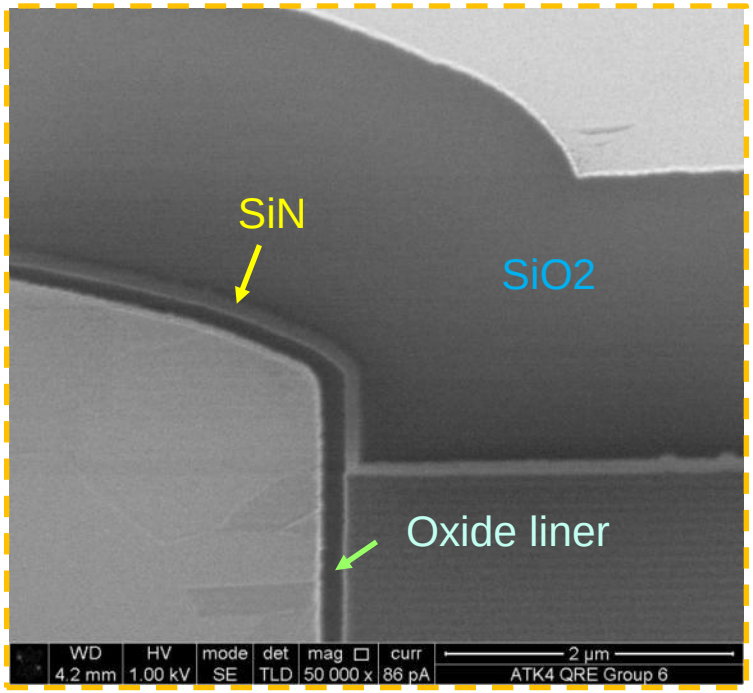
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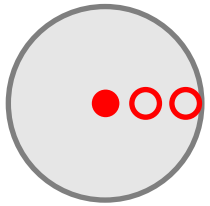
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Dielectric deposition : PECVD







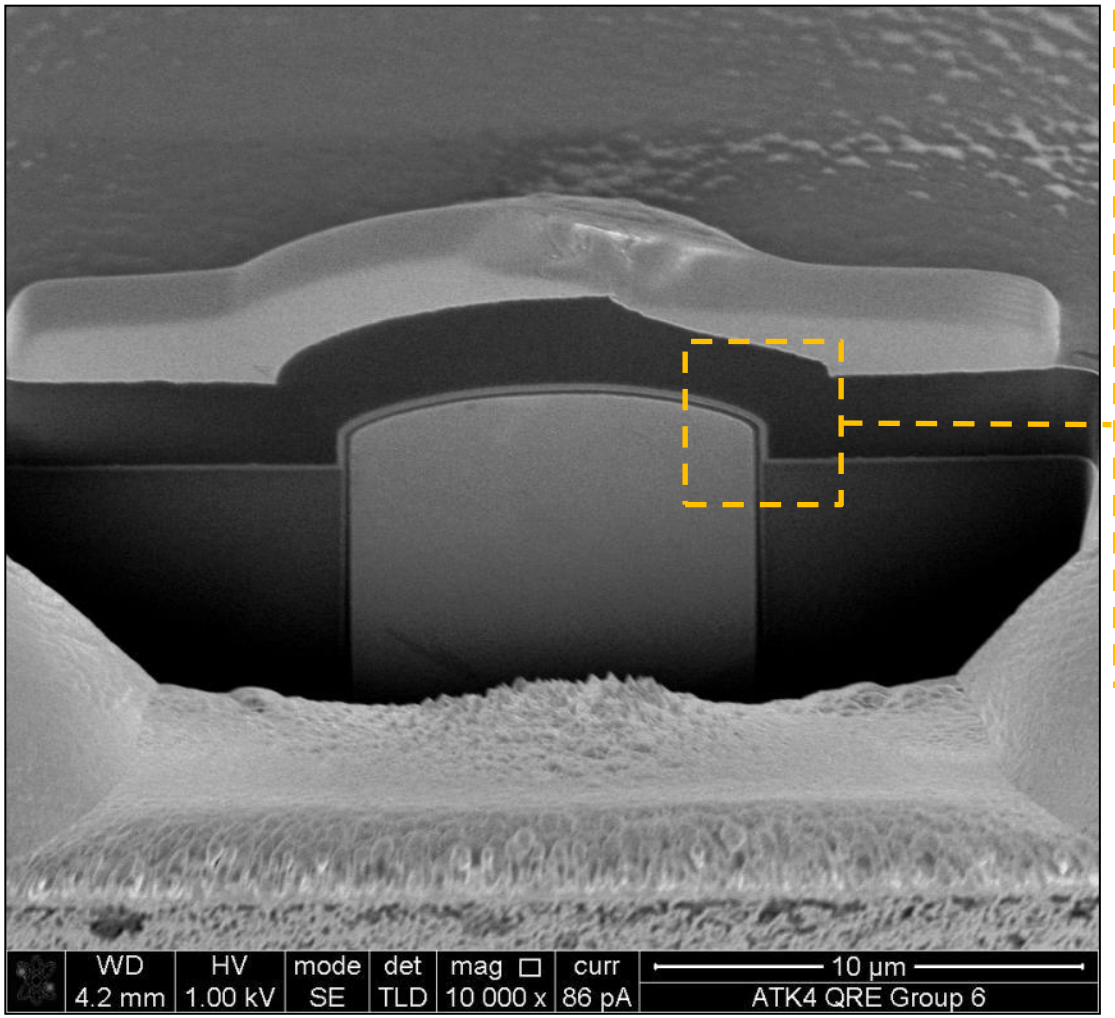
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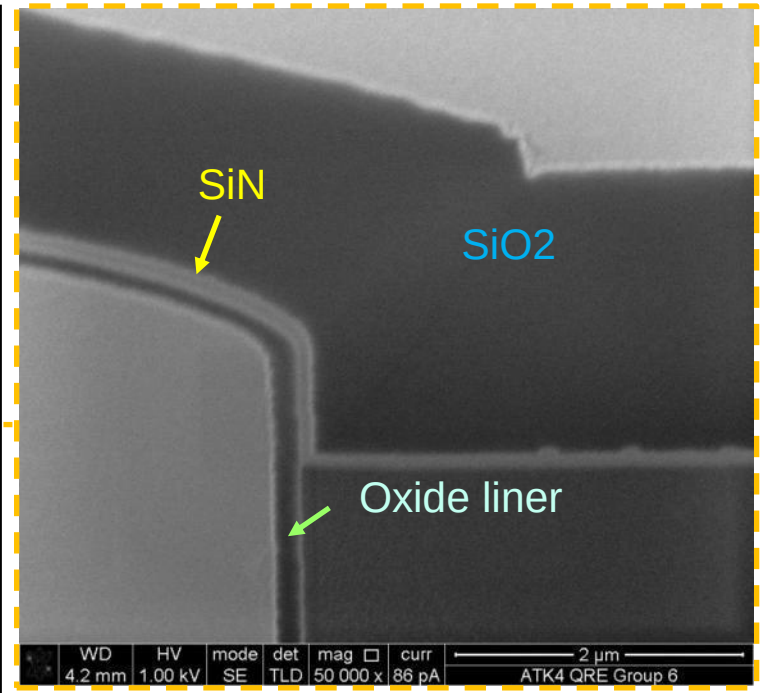
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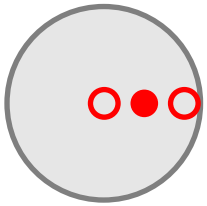
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Dielectric deposition : PECVD







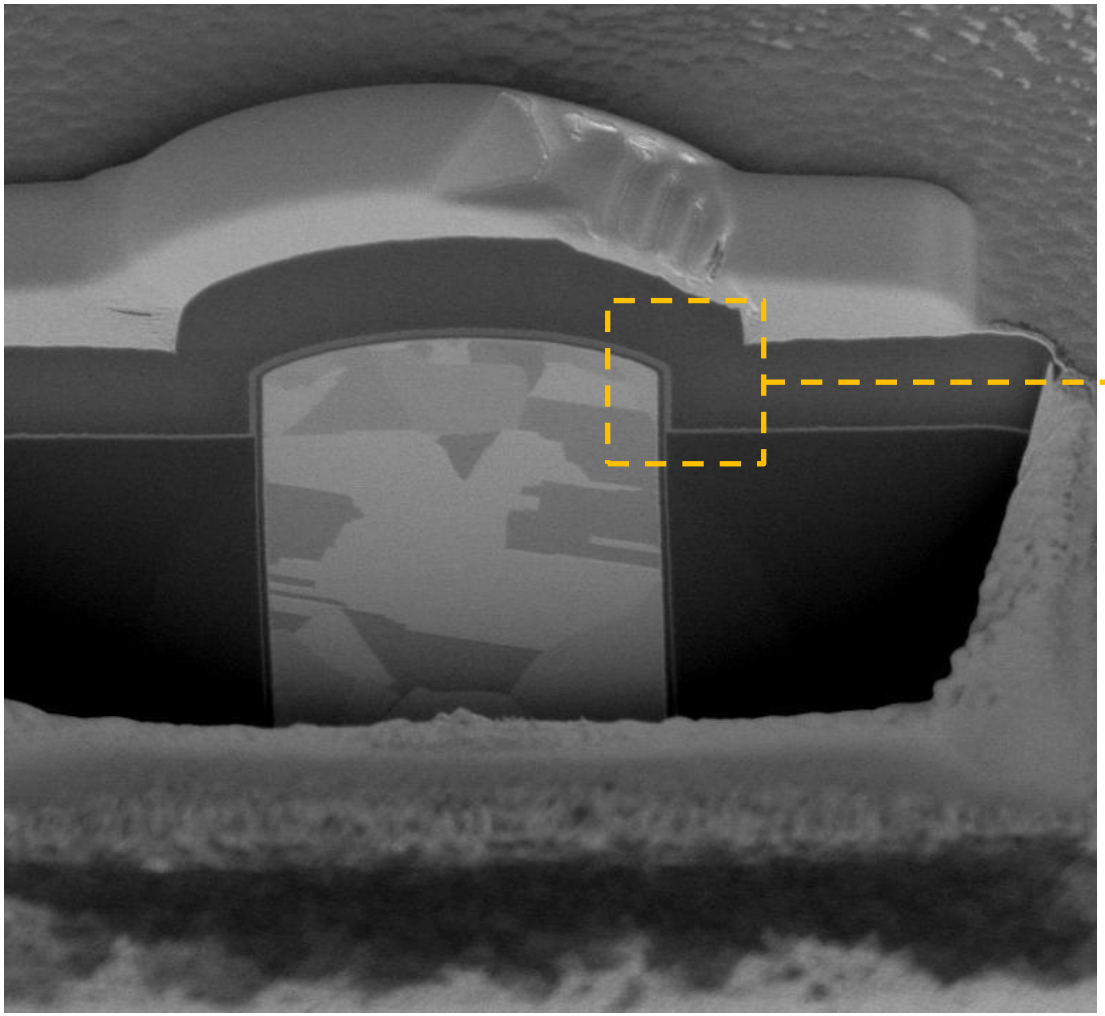
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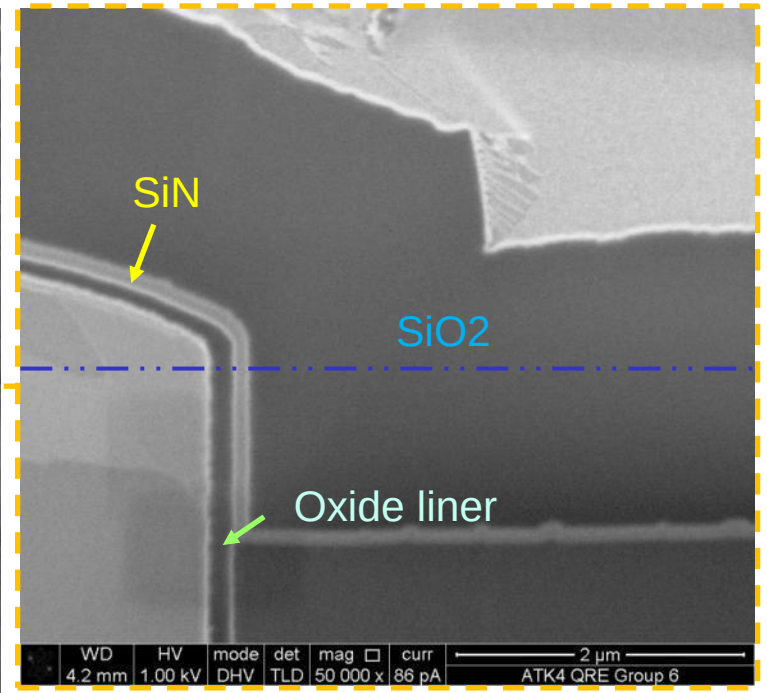
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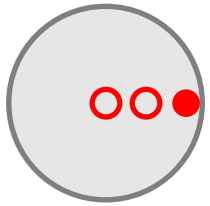
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Dielectric deposition : PECVD







Note

- Found no damage.

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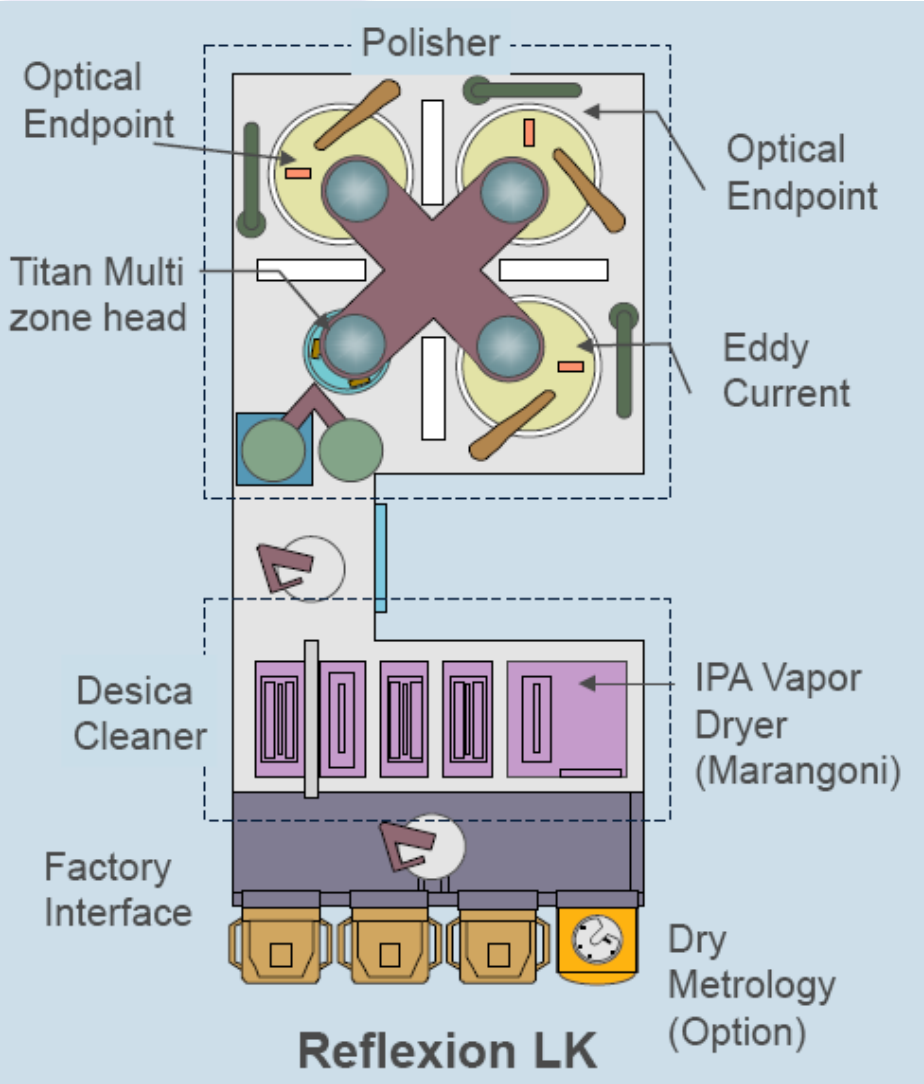
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CMP

- **Process validation**
 - Process optimization to find BKM
 - Oxide/Cu polish process for ISR (Inorganic soft reveal)
 - Si/Cu polish process for flat reveal process
 - Slurry evaluation
 - Post CMP cleaning evaluation

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Secondary reveal : CMP

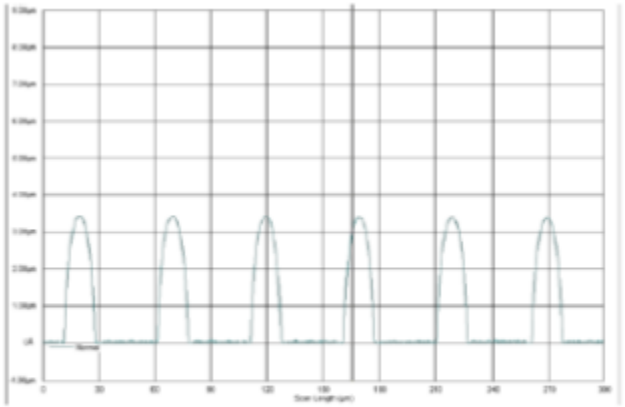


- **Product Features**
 - 3 platen – 4 head polisher
 - Multi zone polishing head
 - In-situ process control optimizes productivity and performance
 - High performance Desica Cleaner
- **Process Controls**
 - Real-Time Profile Control (RTPC™)
 - High-resolution eddy-current endpoint for bulk metal polish step
 - FullScan™ Endpoint
 - Laser endpoint for metal film clearing
 - FullVision™ MX Endpoint
 - Broad-band optical endpoint control for remaining dielectric thickness
 - Si EP/ISPC under development
- **Process BKMs**
 - TSV CMP know-how
 - Low cost/high performance process BKMs for various TSV CMP applications

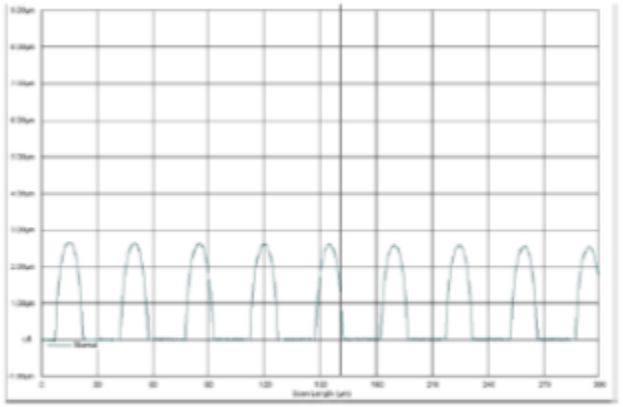
Proven product and industry benchmark CMP tool
>1500 Reflexion/Refelxion LK shipped by 2011

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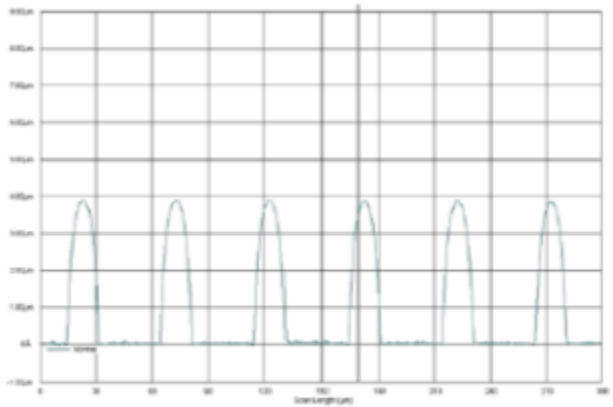
Secondary reveal : CMP



Wafer Center
~3.3um



Wafer Middle
~2.6um

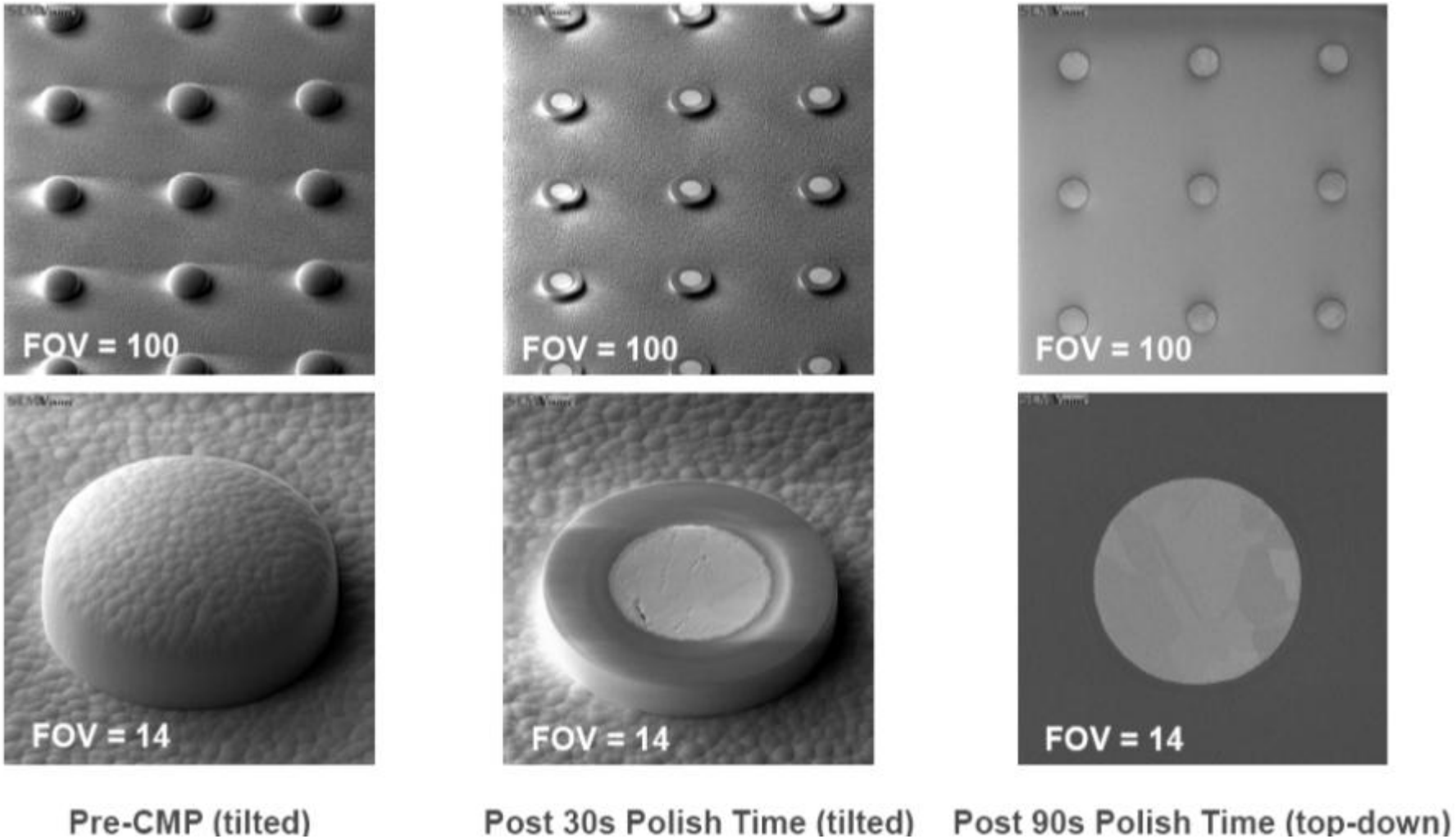


Wafer Edge
~4um

- 1k nitride and 2.8um oxide were deposited on these wafers, pillar height at wafer center and edge post etch are not high enough for CMP to fully exposed copper after pillar planarization and OP with 5k oxide removal on the field.

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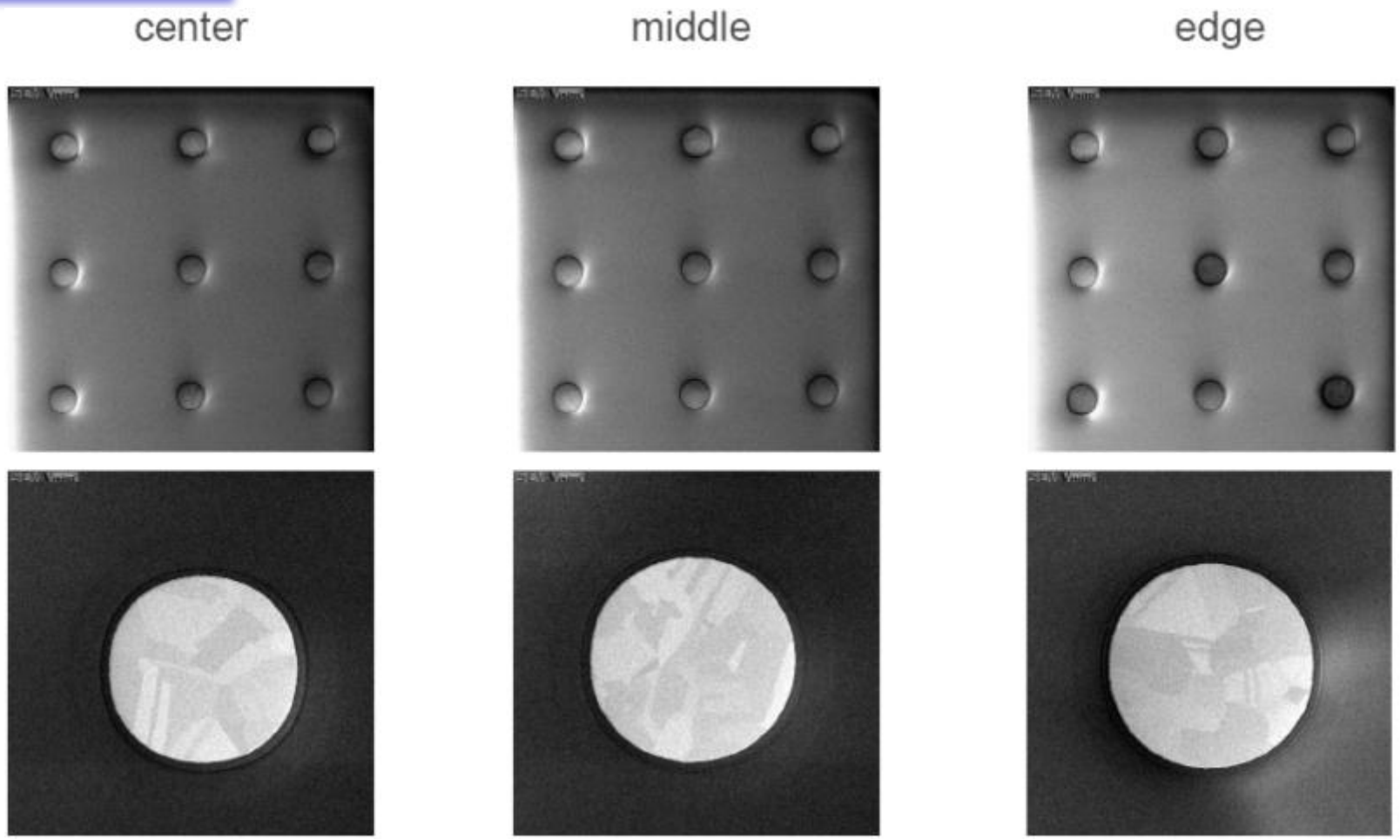
Secondary reveal : CMP



- **Fast and good pillar planarization achieved**
- **Minimum field oxide loss during pillar planaraization**

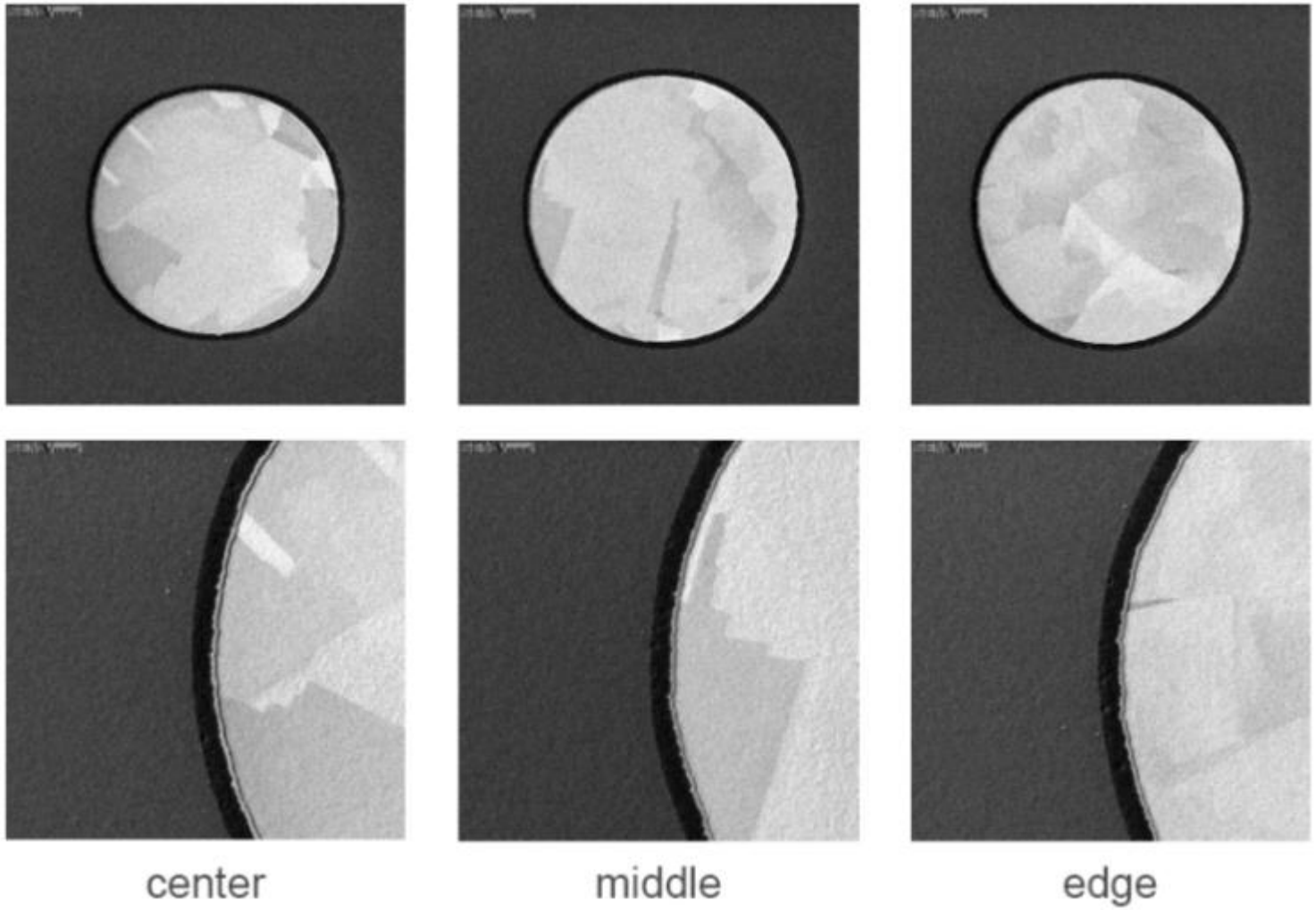
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Secondary reveal : CMP



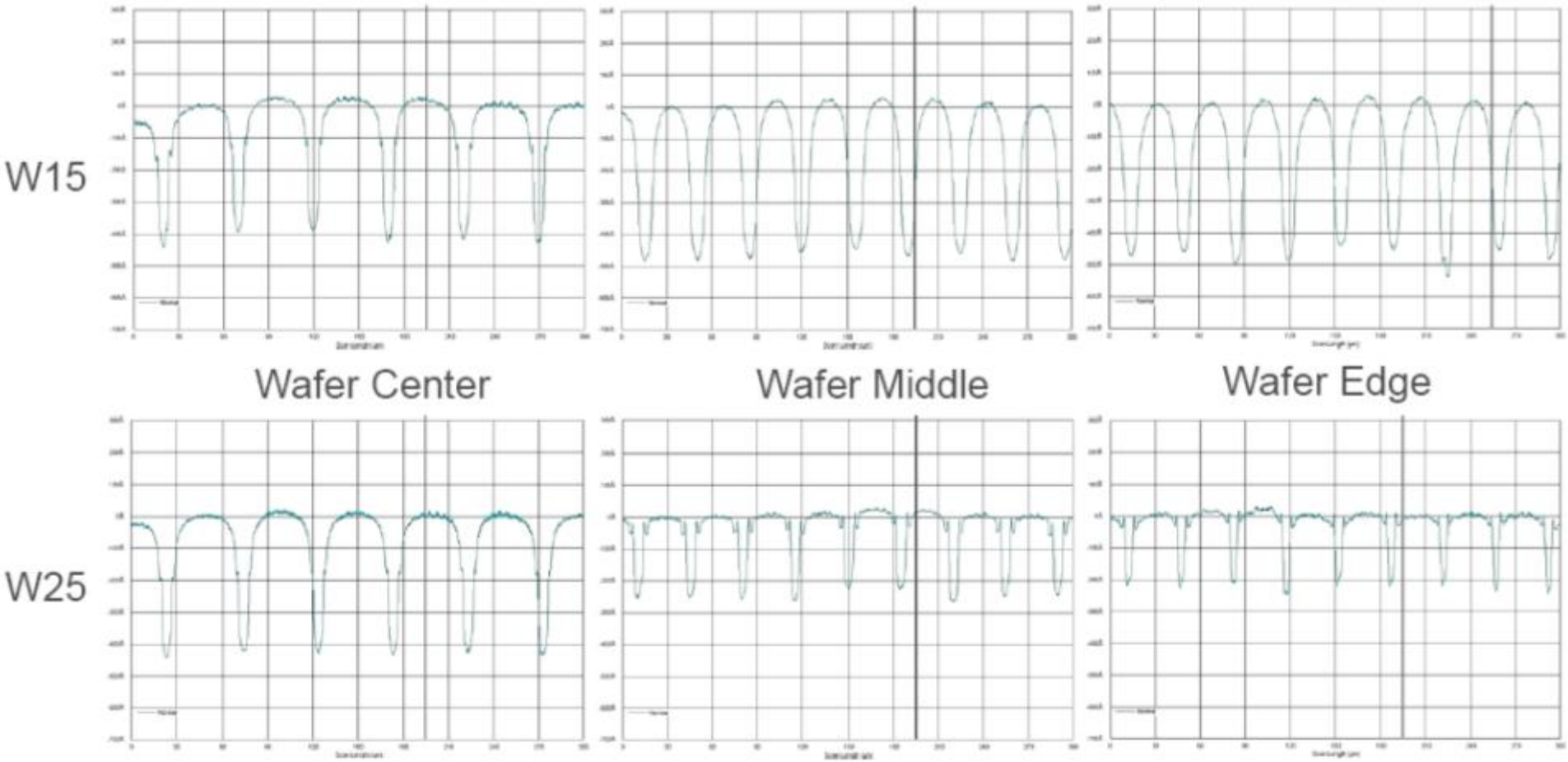
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Secondary reveal : CMP



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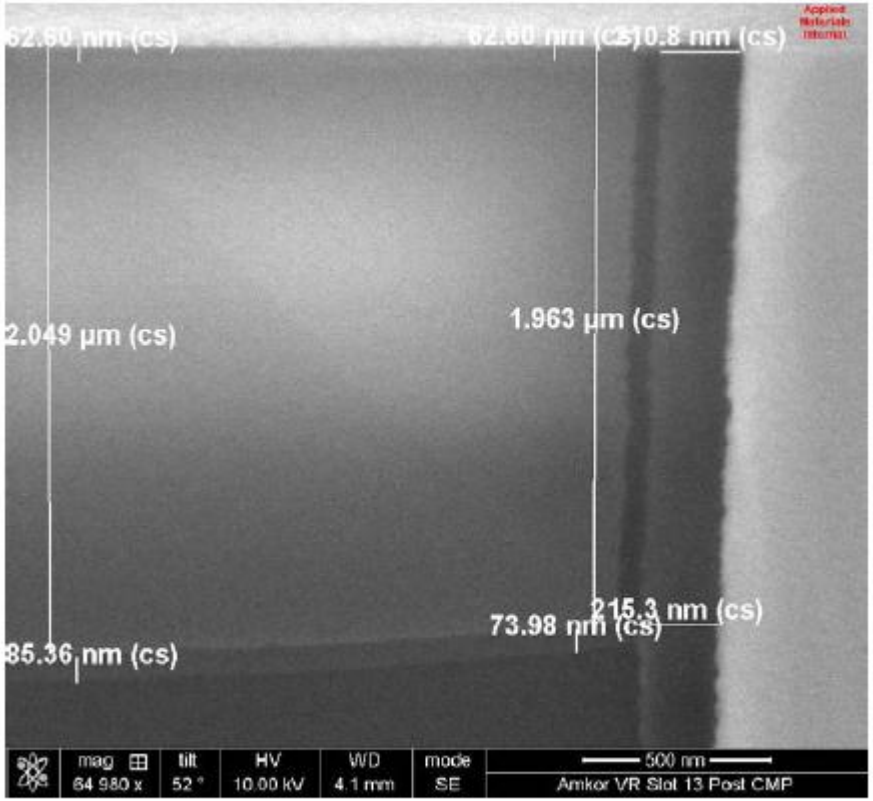
Secondary reveal : CMP
Post CMP Topography



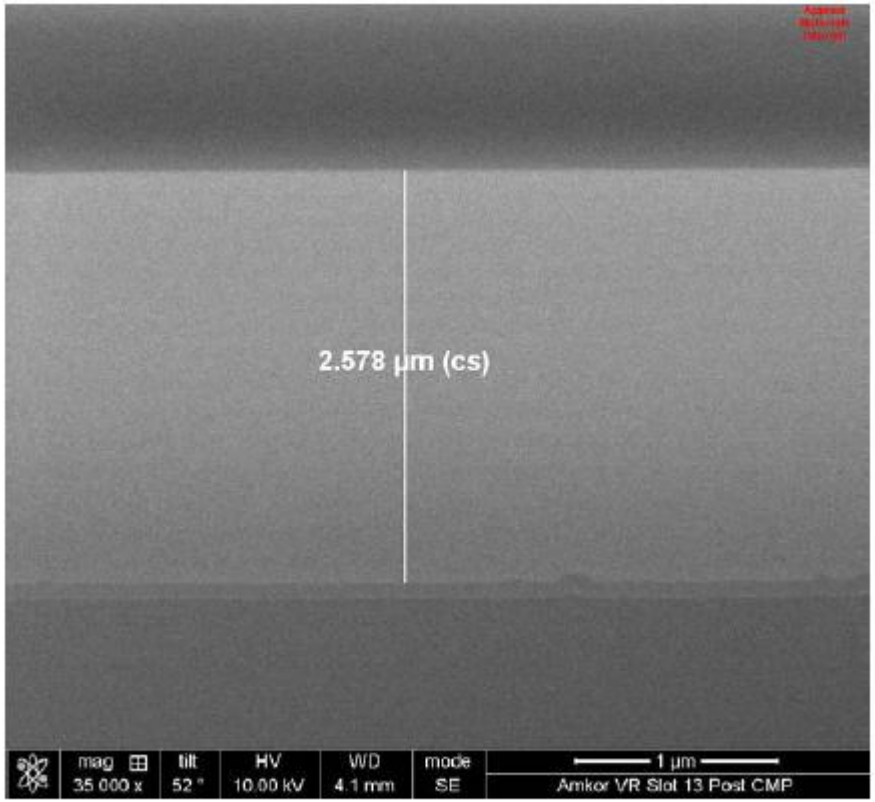
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Secondary reveal : CMP

Layer Thickness confirmation after CMP



Patterned Area Next to Via



Open Field Area

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Stealth Dicing

- **Process validation**
 - Performing SD with wafer frame handling.
 - Evaluation of laser transparent tape.
 - Parameter DOE of laser process
 - Study for auto focus through inorganic passivation

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Stealth Dicing

– **ML300 FH**

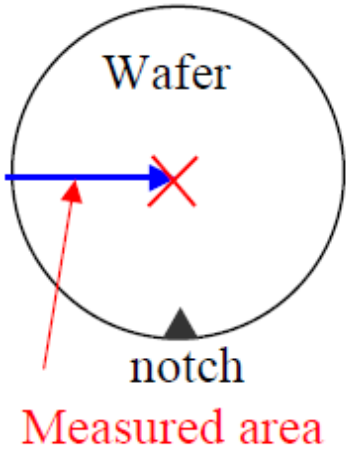
- Frame handling system : full automatic.
- Same system with current K4 tool, except for handler.
- For TSV product.



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Wafer surface flatness comparison

✓Observed wafer BG tape laminated by manual process



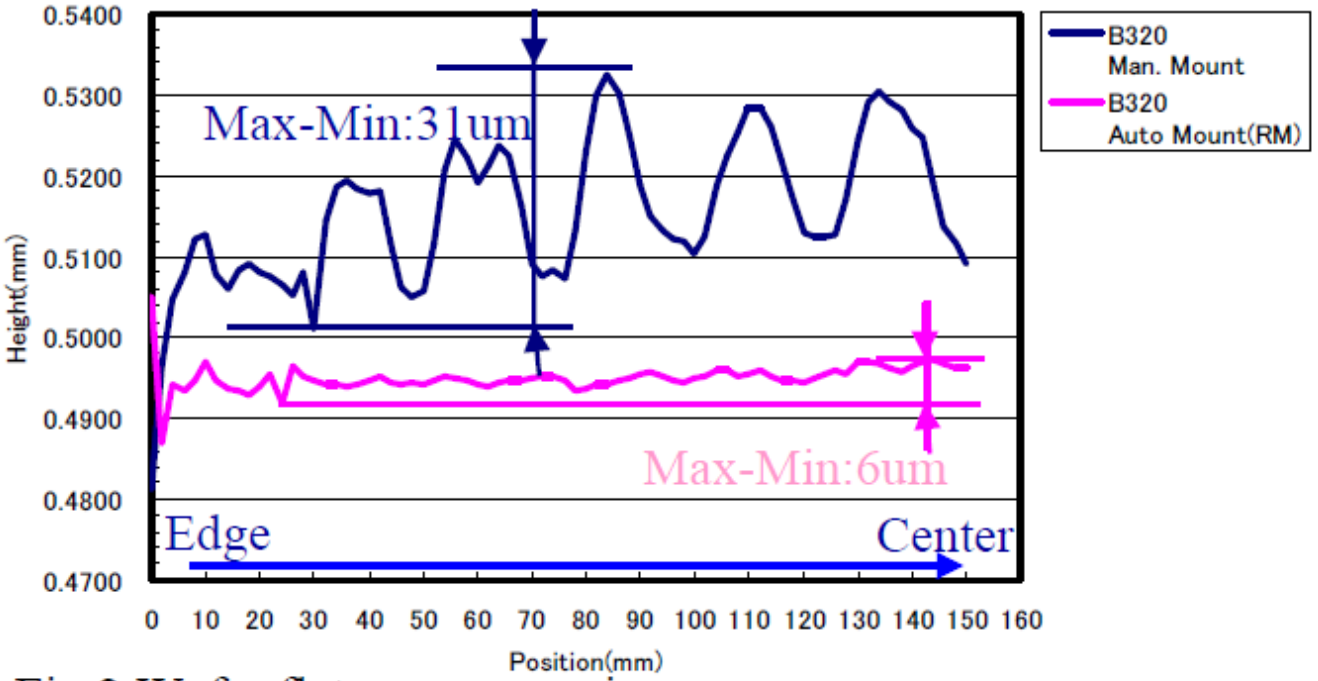


Fig.2 Wafer flatness comparison

Result

Wafer flatness was much improved after optimize tape laminate condition.

With improved condition, can expect stable Auto Focus result

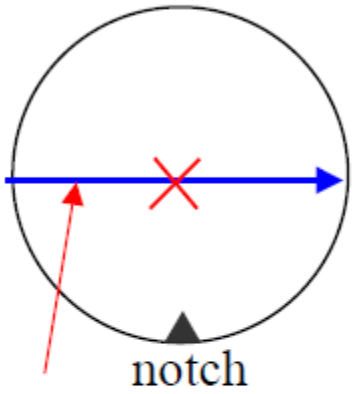
= stable cutting quality.

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Investigation for too low SFV on SiN layered wafer

✓Measured SFV on dicer



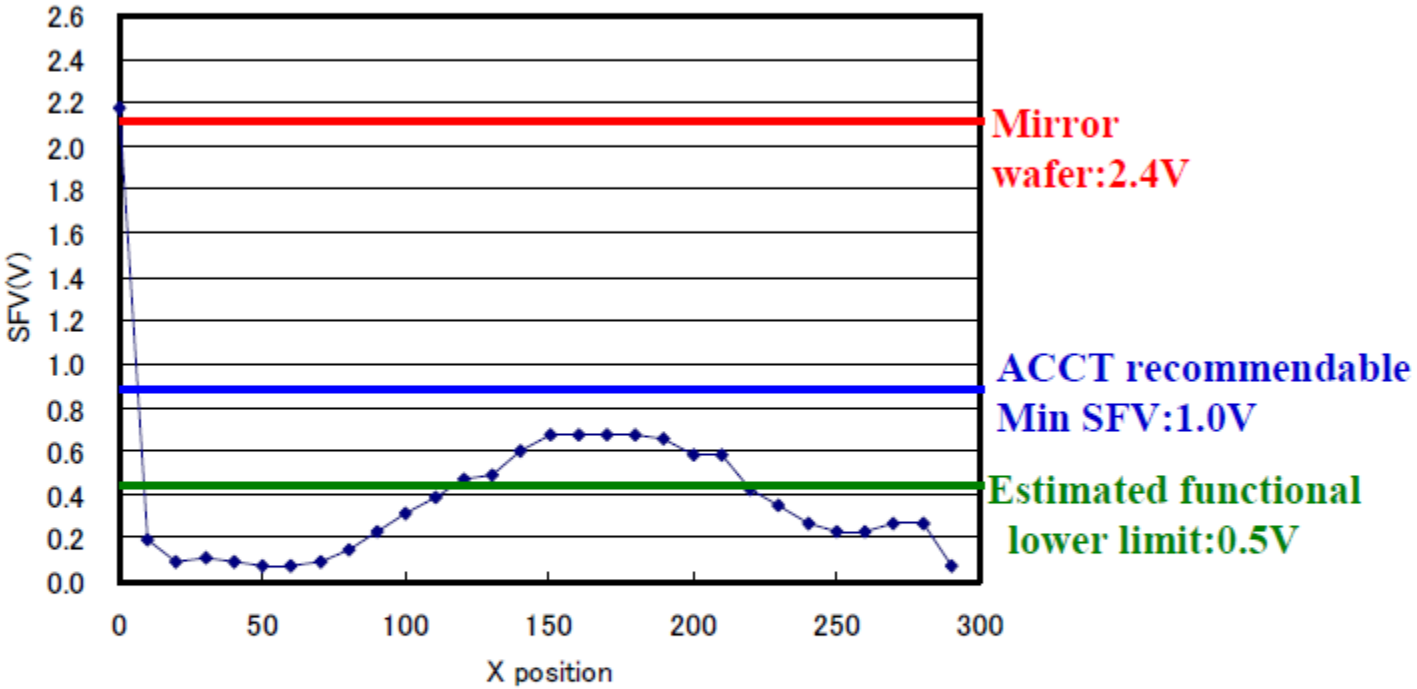


Fig.3 SFV check result

Result

SFV was very low at all the point on wafer.

It was around “0.1V” at the lowest case.

*SFV is same as quantity of reflected AF laser from wafer surface.

*Enough high SFV (=enough reflectivity) is required to keep good Z-accuracy

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Influence of SiN layer on wafer surface

✓ Simulation result f reflectivity and suspected root cause of too low SFV

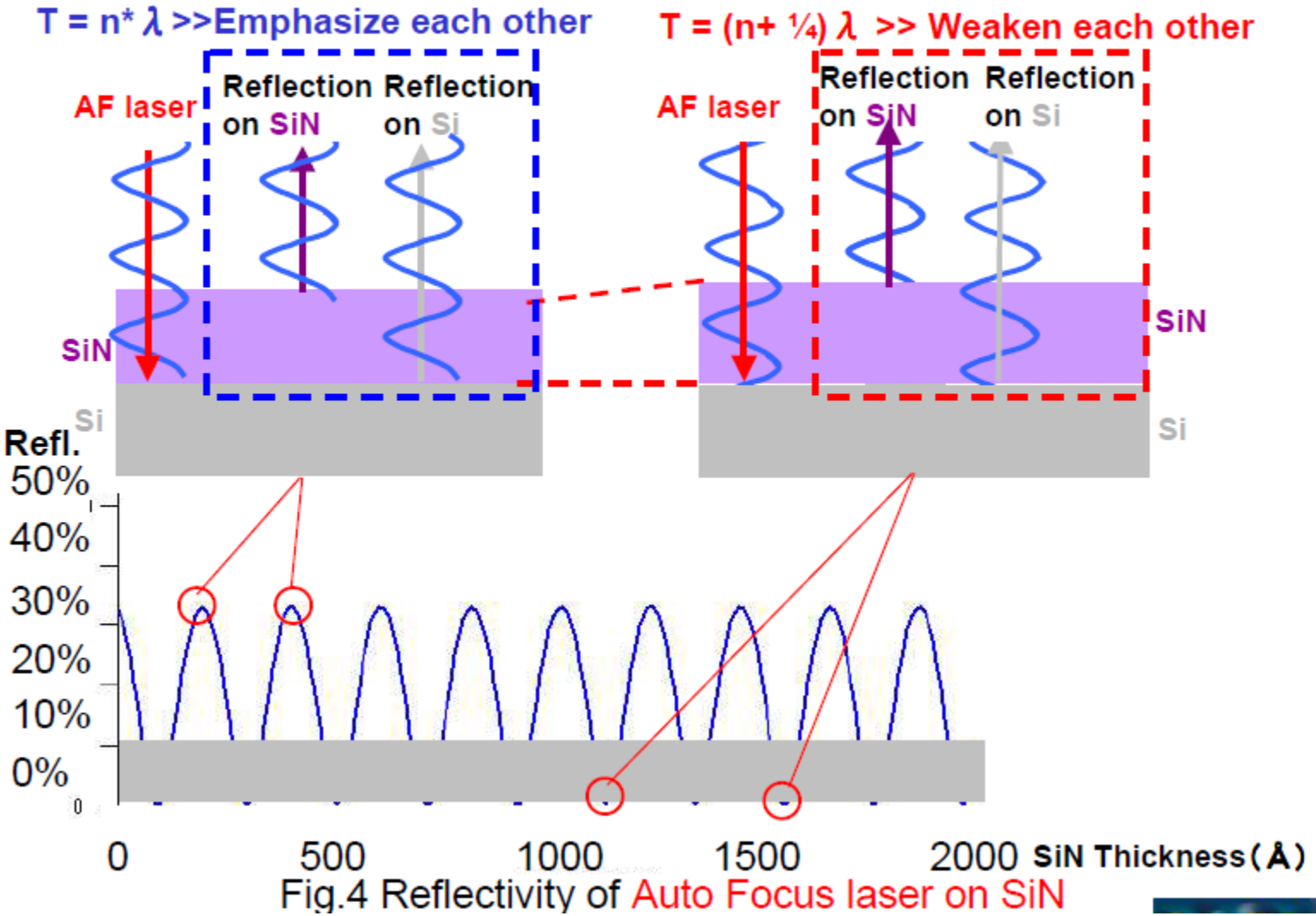
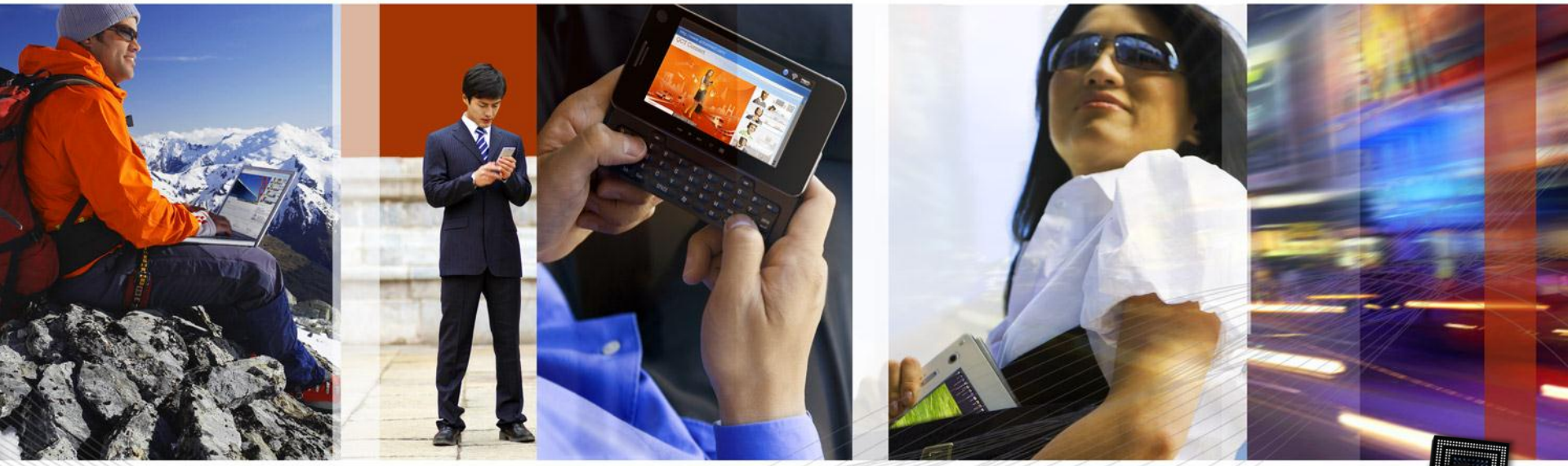


Fig.4 Reflectivity of Auto Focus laser on SiN

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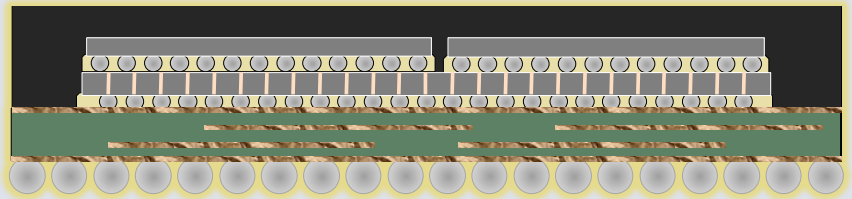
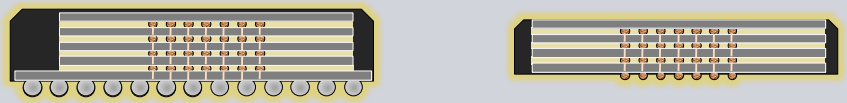
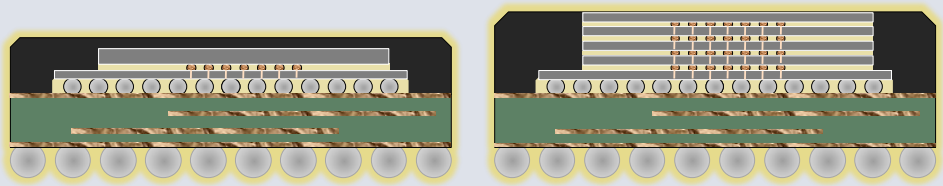
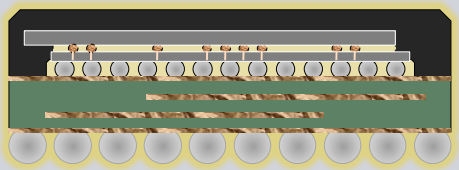
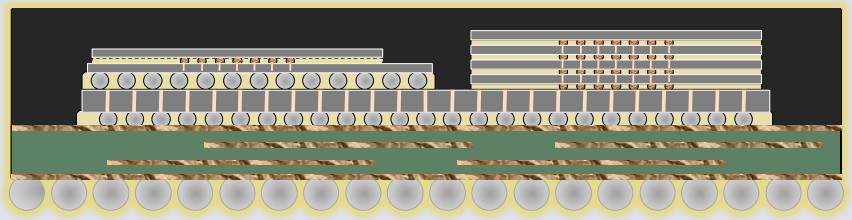
REDEFINING MOBILITY

Roadmap for Design and EDA Infrastructure for 3D Products

Riko Radojcic
Qualcomm
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Tel : 1 858 651 7235

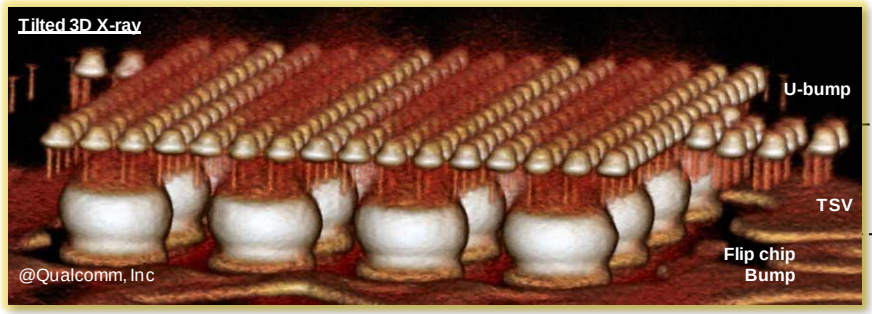
HotChips 2012
Cupertino, CA
Aug 2012

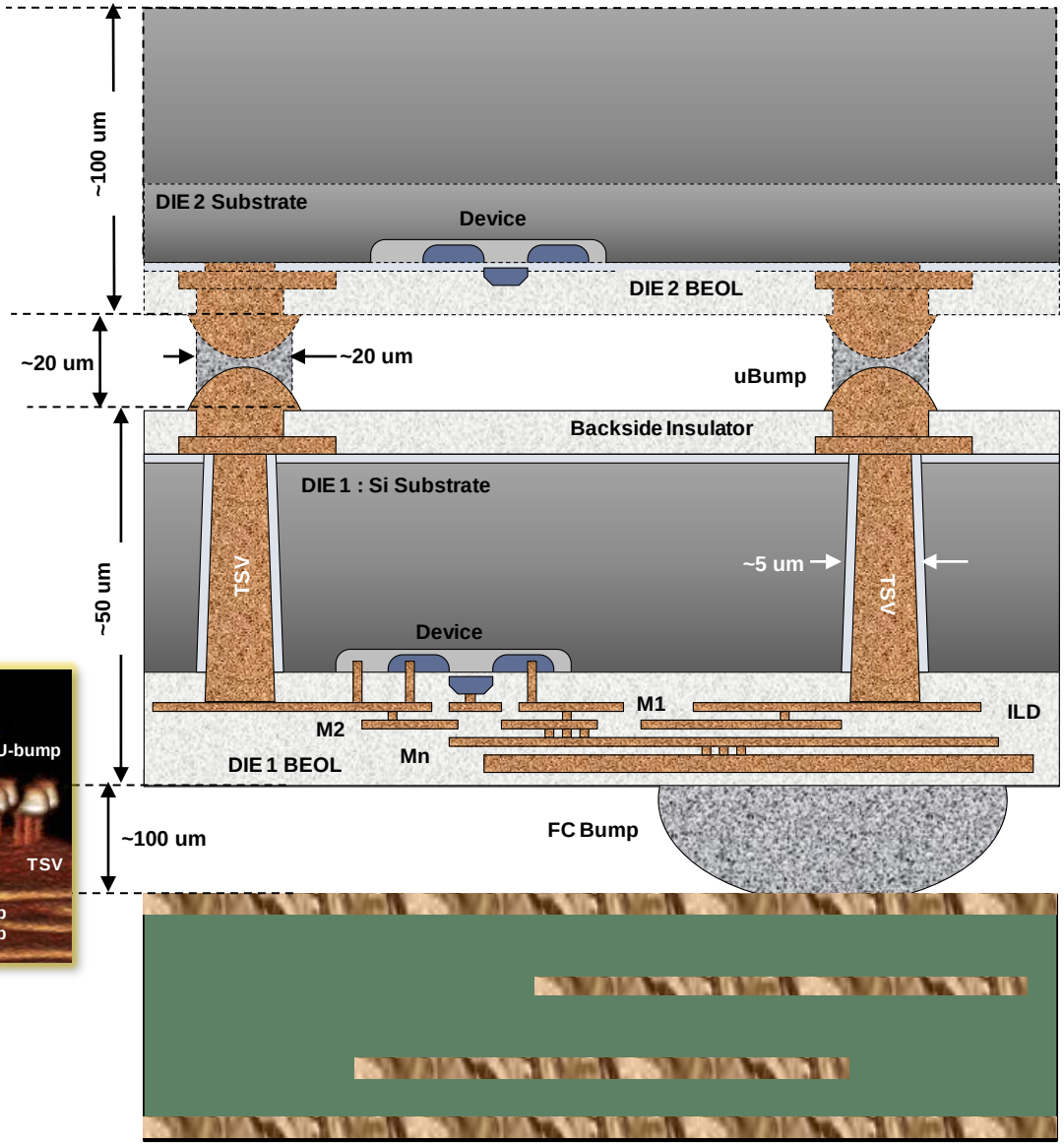
Some of the Typical 3D Options

2.5D	Side by side die stacked on a passive interposer that includes TSVs	
3D Memory	Multiple DRAM die stacked standalone or on an active interposer	
3D Memory on Logic	One or More DRAM die stacked directly on logic die (M-0-L)	
3D Logic on Logic	Multiple logic die stacked on top of each other (L-o-L)	
3D + Interposer	Mix of side by side and stacked schemes with a passive or active interpsr	

Evolving to “Mainstream” 3D Technologies

- For 3D stacking
 - e.g. Wide IO Memory on Logic
 - stacking orientation: F2B
 - TSV via diameter ~ 5u
 - wafer thickness ~ 50
 - uBump Array pitch : 40x50



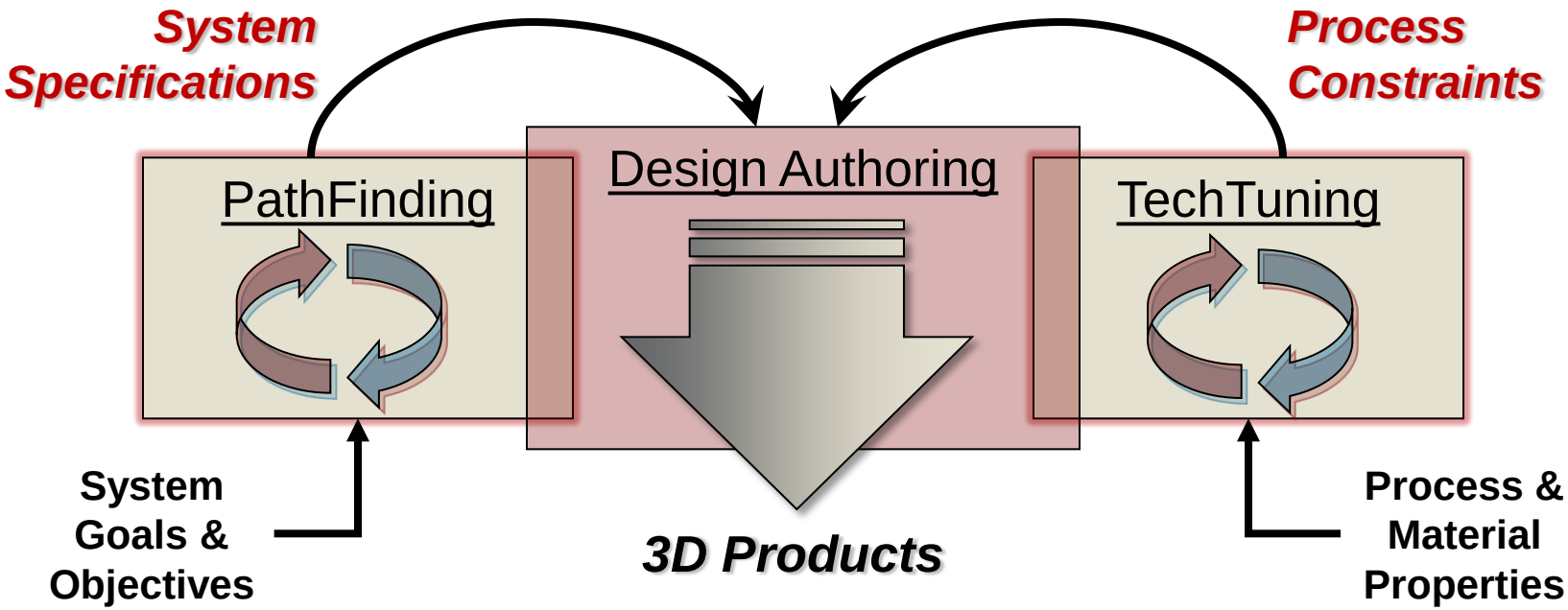


Snapshot of Intrinsic Technology Status

	Was (common concern a few years ago)	Is (our take)
Process	High aspect ratio (10:1) 5/50 TSV process	✓
	Thinning & Backside wafer processing	✓
	Microbump and Joining	✓
	Integration & Stacking	✓
	Intrinsic Reliability Assessment	☛ in flight
	Standards (JEDEC, SEMI, Sematech, 3D EC, …)	☛ in flight
Design (M-o-L)	EDA tools (for "2D-like" Memory-on-Logic design)	☛ mostly
	Design Enablement (for "2D-like" Memory-on-Logic design)	✓
	Testability (for "2D-like" Memory-on-Logic design)	✓
	Variability (Corner for "2D-like" Memory-on-Logic design)	✓
	Standards (JEDEC, Si2, IEEE …)	☛ in flight
Product	System Level Value Proposition	✓
	Thermal Modeling & Design for Thermal	☛ in flight
	Stress Modeling & Design for Stress	✓
	SI modeling & Design for Parametric Yield	✓ in flight
	Cost Structure & Business Models	TBD
	Yield and Yield Learning	TBD
	Volume Manufacturing Ramp	TBD

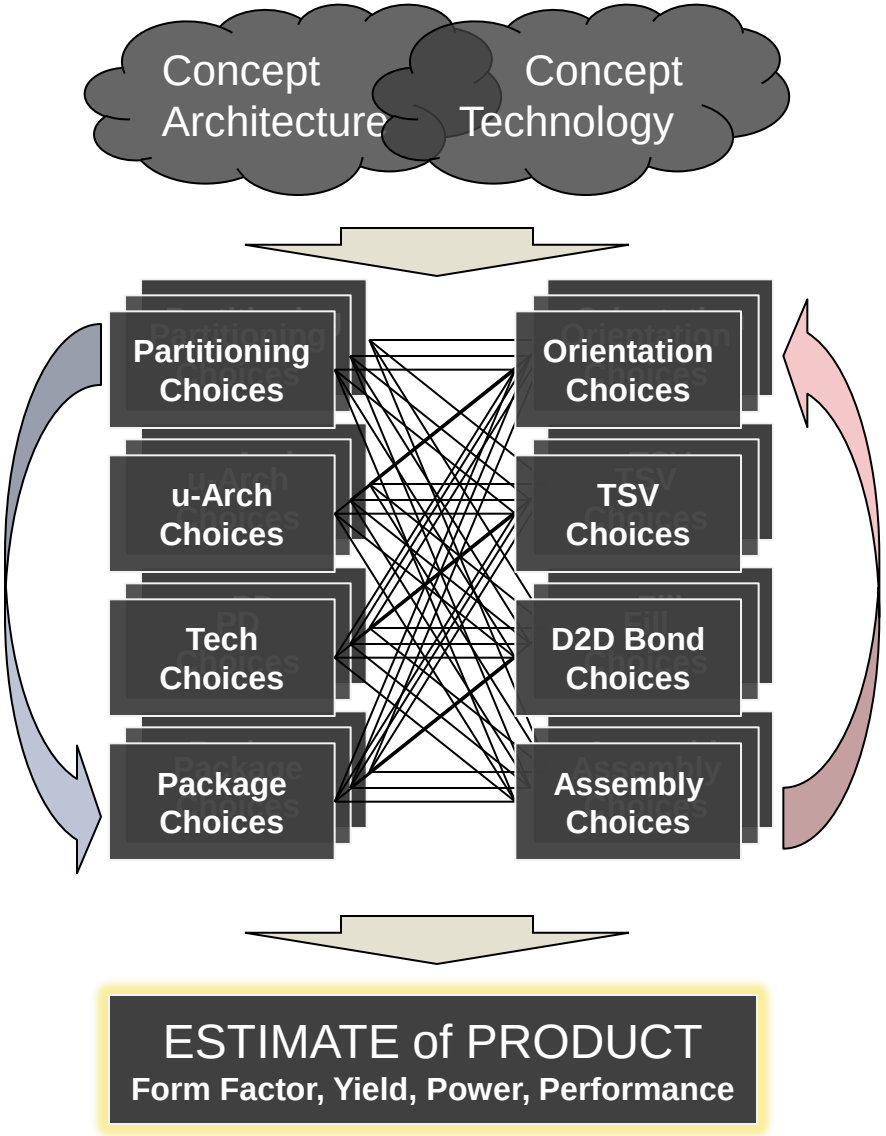
Eco-System for 3D Design

- **Segment Design Eco-System into 3 Buckets to Address 3 Key Challenges**
- ***Design Authoring* – actual chip design**
 - Implement Design via (mostly) Traditional 2D Chip Design Flow (RTL2GDS))
 - Output GDS
- ***PathFinding* – design/technology concept exploration**
 - *Manage Choices* via Cheap, Quick & Dirty Concept Design
 - Output Clean Specs
- ***TechTuning* – physical space exploration**
 - *Manage Interactions* via Cheap, Electrical, Thermal & Mechanical Chip Simulation
 - Output Clean Constraints



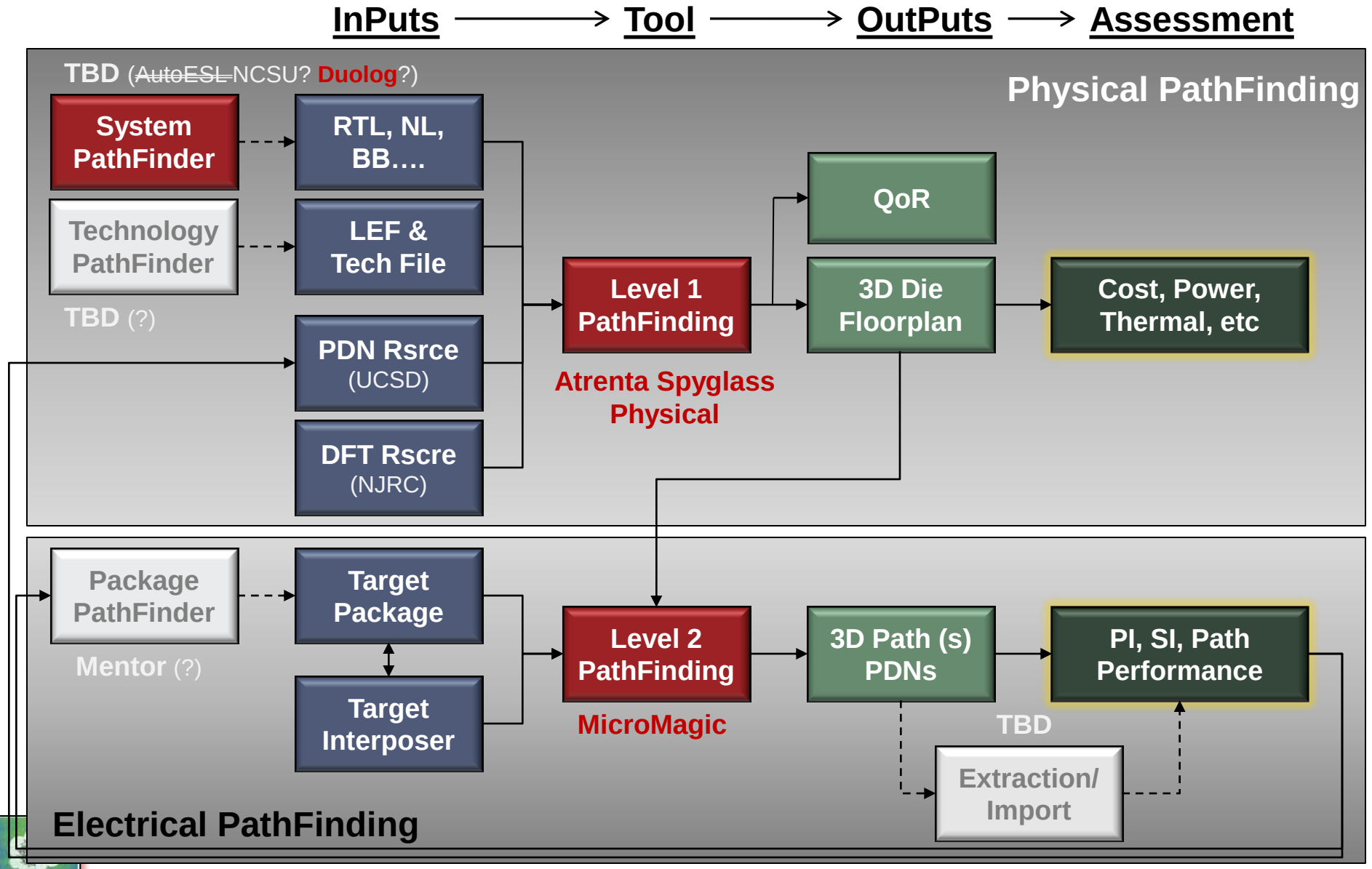
PathFinding: Why & What ?

- Managing Choices ….
 - Want to optimize product attributes
 - Cost, power, performance, engineering …
- Need to Co-Optimize Process & Design
 - Winning 3D Product will Be Architected specifically to Leverage 3D Technology
 - Selection of choices is Product Specific
- In General: Need Spatial Awareness
 - Quick and flexible
 - Hi fidelity vis-a-vis accuracy
- For 3D : Also Need Heterogeneity
 - Multiple stacking styles & orientations
 - Multiple tech files
 - Multiple levels of hierarchy
 - Multiple resource constraints
- Structured Methodology.
 - Past experience not applicable
 - Opportunity for paradigm shifts
 - Not tied to Legacy design
 - Process-Design-Package co-optimization



Details :3D System Integration, Springer 2011

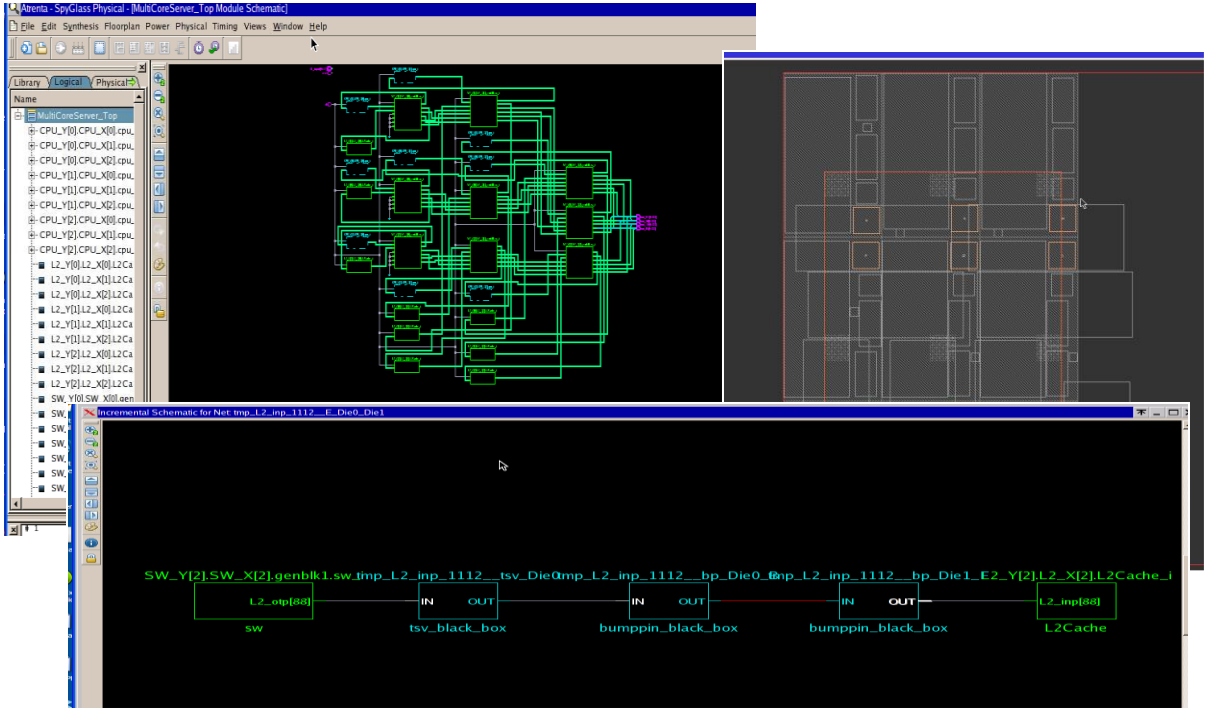
3D PathFinding : Current View

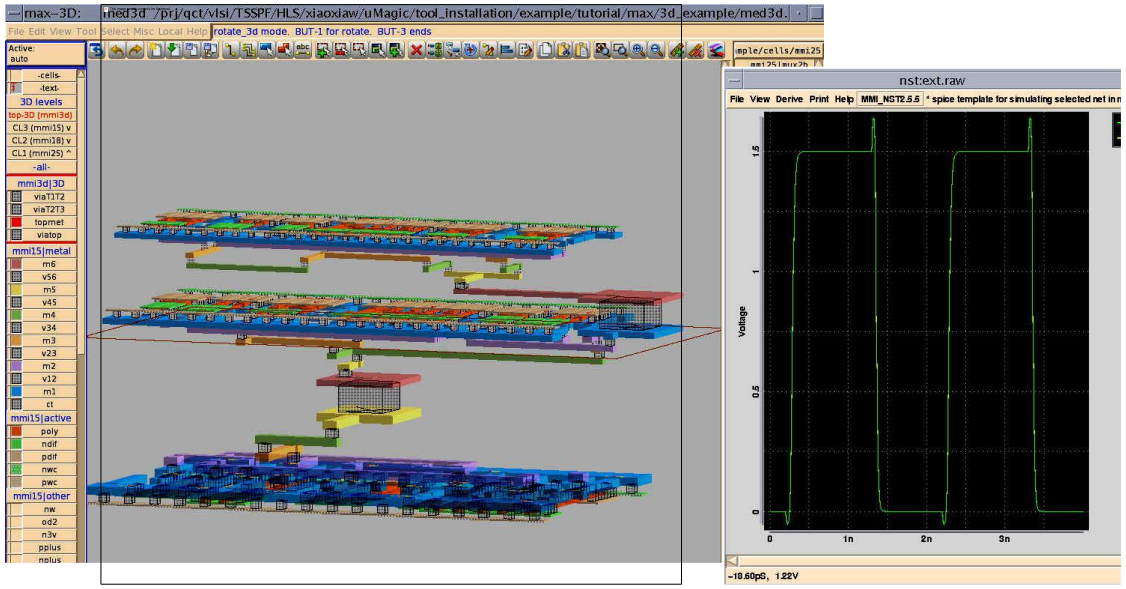


ATRENTA
Micro Magic
UC San Diego
Local Impact, National Influence, Global Reach
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PathFinding

- Level 1 (Atrenta): think
 - RTL & Netlists
 - Block Level Schematics
 - Partitions
 - Block assignments
 - T2T connectivity
 - Global Routing
 - Floorplans
- Level 2 (MicroMagic): think
 - Transistor Level Schematics
 - T2T layout
 - SPICE Netlist
 - Waveforms
 - Polygons
 - GDS





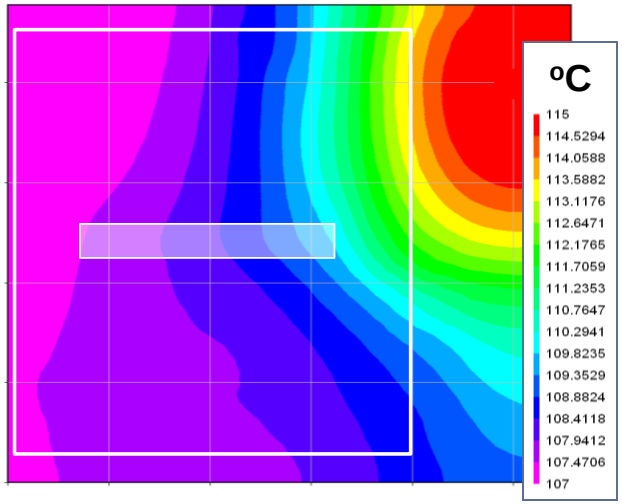
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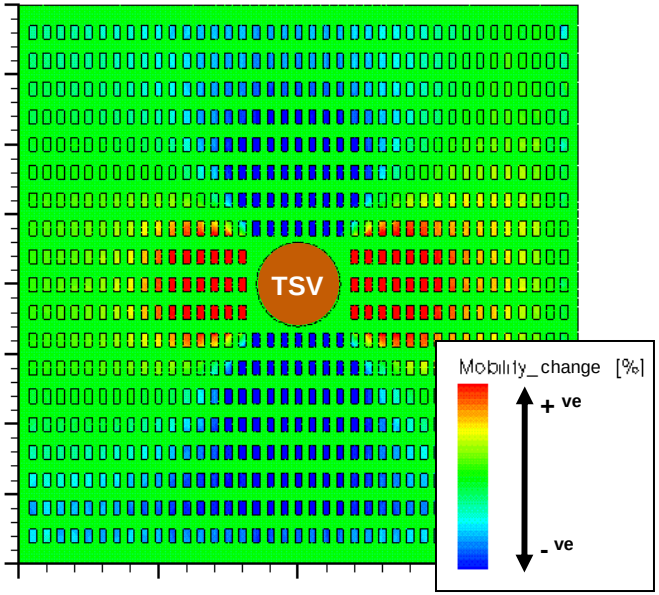
Micro Magic

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TechTuning: Why & What ?

- Managing Interactions
 - Intimate Proximity and Coupling Between Die
 - In Electrical, Thermal & Mechanical Domains
- Electrical Domain Interactions
 - Within Die Interactions with New Features
 - Substrate noise, Coupling etc..
 - Die to Die interactions (SI, PDN, PI…)
- Thermal Domain Interactions
 - Within a Die & Die to Die
 - Need Thermal Rules & Guidelines
 - Design Specific & Technology Specific
 - Need a methodology to plug into std design flow
- Stress Domain Interactions
 - Within a Die & Die to Die
 - Need Thermal Rules & Guidelines
 - Design Specific & Technology Specific
 - Need a methodology to plug into std design flow



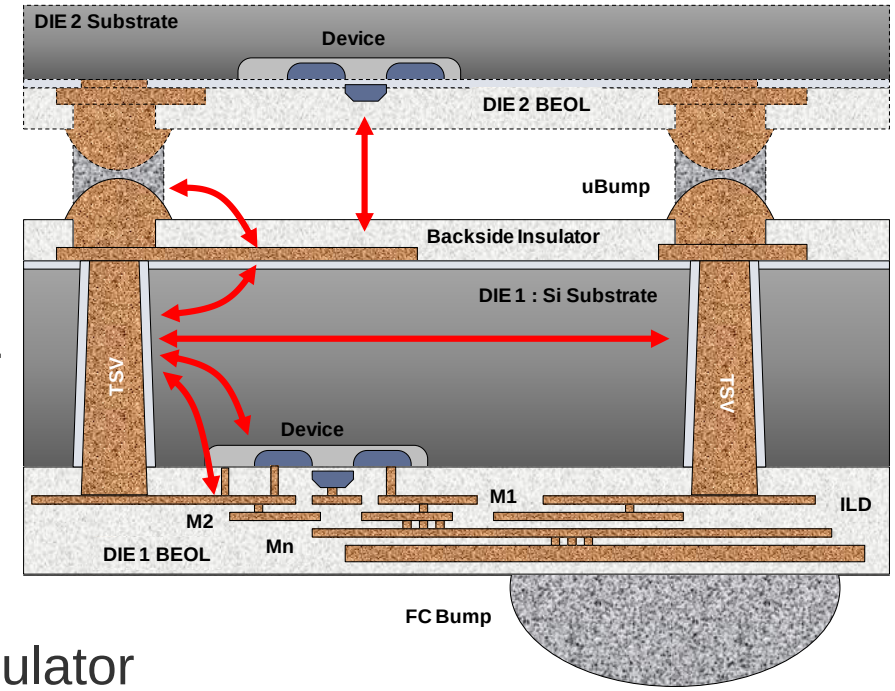


Details :3D IC Stacking Technology, McGraw Hill 2011

cadence® SYNOPSYS® Mentor Graphics® QUALCOMM CDMA Technologies

3D Electrical Interactions

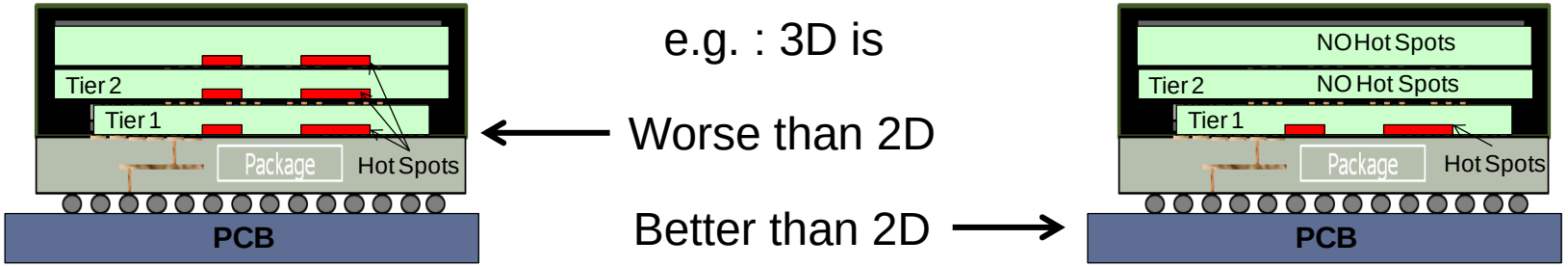
- Many Possible Interactions
 - Die to Die – close proximity
 - Within a Die – new features



- New Geometries: not just simply planar
 - uBump to BRDL
 - TSV to BRDL
 - TSV to TSV
 - TSV to M1
- New Features: not just conductor or insulator
 - MOS nature of TSV & Semiconductor nature of Si
 - e.g. Substrate Noise Coupling: TSV to Device
 - vs. substrate thickness
 - vs. Doping Profile in the Si substrate
 - vs. TSV to Device Separation
 - vs. Substrate Tap & Guard Ring Configuration
 - etc…
- Need true 3D Chip Level Extraction & Coupling Analyses
 - Or a restricted layout with pre-characterized macro model

Thermal Challenges => a Fundamental Constraint

- Thermal: a Global (=System Level) & Local (=Component Level) Challenge
 - Global Concern : must manage skin temperature and overall system power
 - Local Concern : must manage hot spots, junction temperature, and power density
 - Compounding Factor: all advanced systems use some form of Thermal Mitigation
- Thermal is not a 3D-only Challenge
 - A Problem that has to be addressed with 2D Components as well…
 - At Architecture, Design, Floorplanning, Packaging, Application, Software …
 - Could be a 3D Opportunity ?



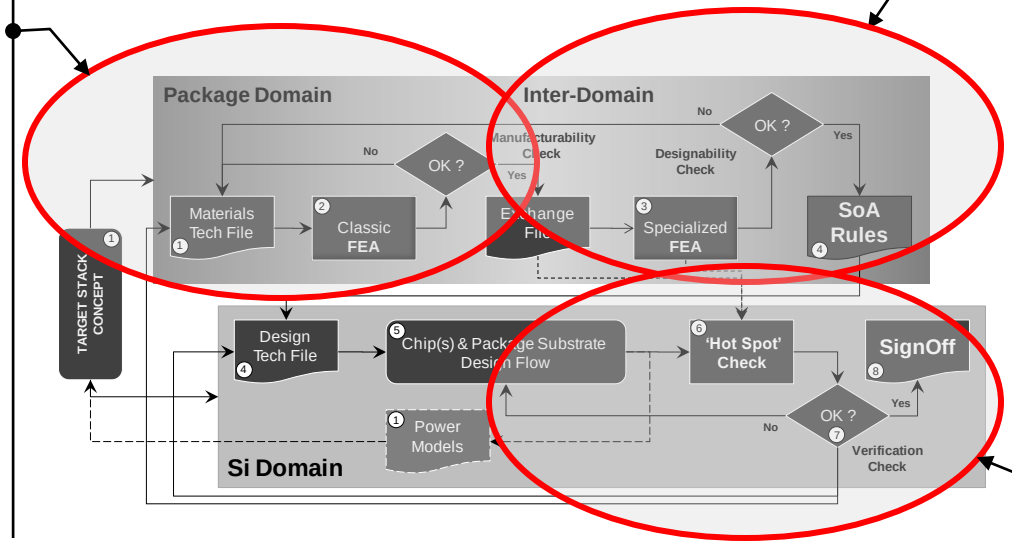
- Need a System-Chip Co-Design Methodology & Tools
 - Faster and More Flexible than the traditional CFD / FEA methodologies
 - Compatible with cross – company handshake (a la TDP practice in PC domain)
 - Compatible with fuzzy PathFinding-like forward looking inputs
 - Compatible with different system level ‘knobs’
 - Compatible with different chip level ‘knobs’

Implementation of a TechTuning Flow for Stress

- Interface to actual Design Authoring : **Rules now**
 - maybe in-flow model based simulation later..
 - Based on ‘off-line’ simulations using specialized tools
 - Define a ‘Safe Operating Area’ => a set of rules
 - Supplement with a smart ‘hot spot’ checker to close the loop

Traditional Simulation

✓FEA methodology
✓~1 to 0.01mm range
✓Hosted Model from AMKOR
✓Working on similar deliverable from ASE



Specialized Simulation

✓Submodeling & specialized FEA methodology
✓ μm to nm range
✓SNPS FAMMOS tool

“Hot Spot” Checker

- Validation that bits and pieces fit & SIGN OFF the design
- Must interface to design environment : I/P : GDS2 , LEF, DEF …
- May have to be COMPACT MODEL Based (read the whole design and include all effects)
- Working with MENT

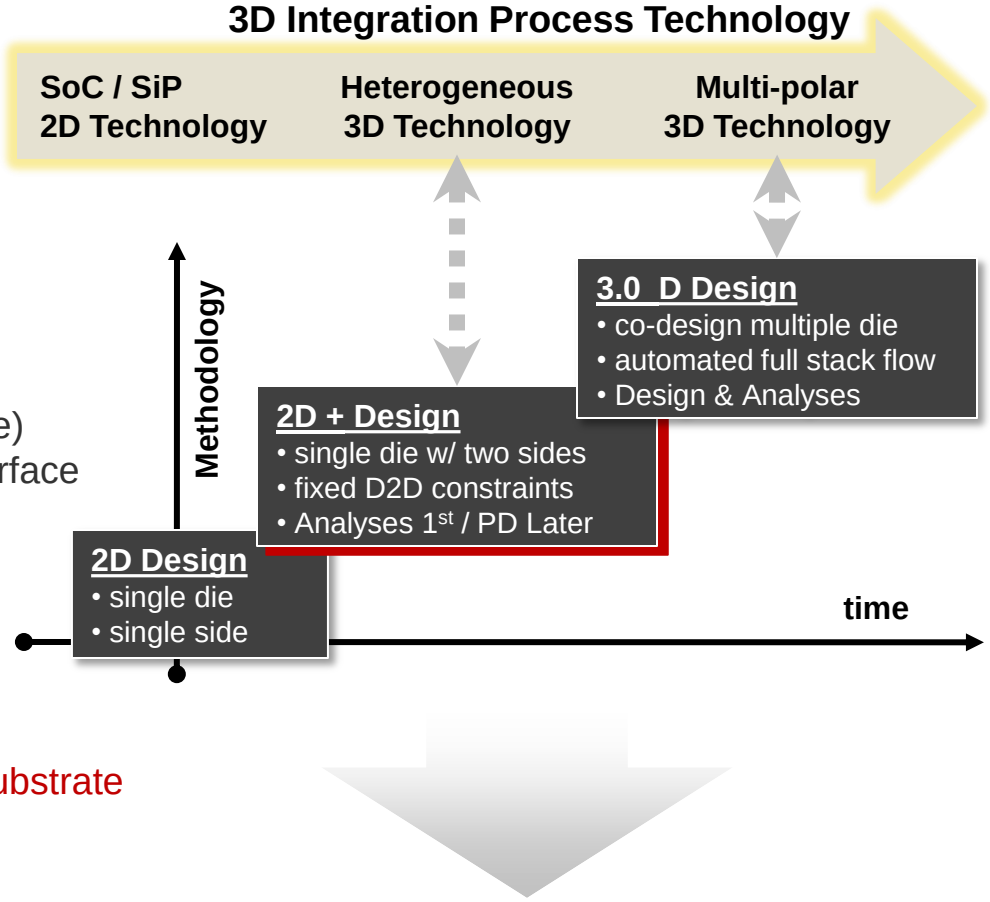
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Managing Costs : What Does It Mean for TSS Design?

- Expect Gradual and Graceful Evolution
 - Process and Design – together / in synch
 - Significant investment in the existing flow
 - Will be Applications Driven

- Now : Heterogeneous Stacking
 - e.g. Memory (or Std Analog) on logic
 - Design Methodology Requirements
 - Partitioning : by die types w/ spec interface
 - Syntheses : 1-die-at-a-time
 - Floorplanning : constraint from the other die
 - Physical Design : partial 2-sided die (maybe)
 - Physical Verification: 1-die-at-a-time + interface
 - Analyses : whole stack (eg PDN)

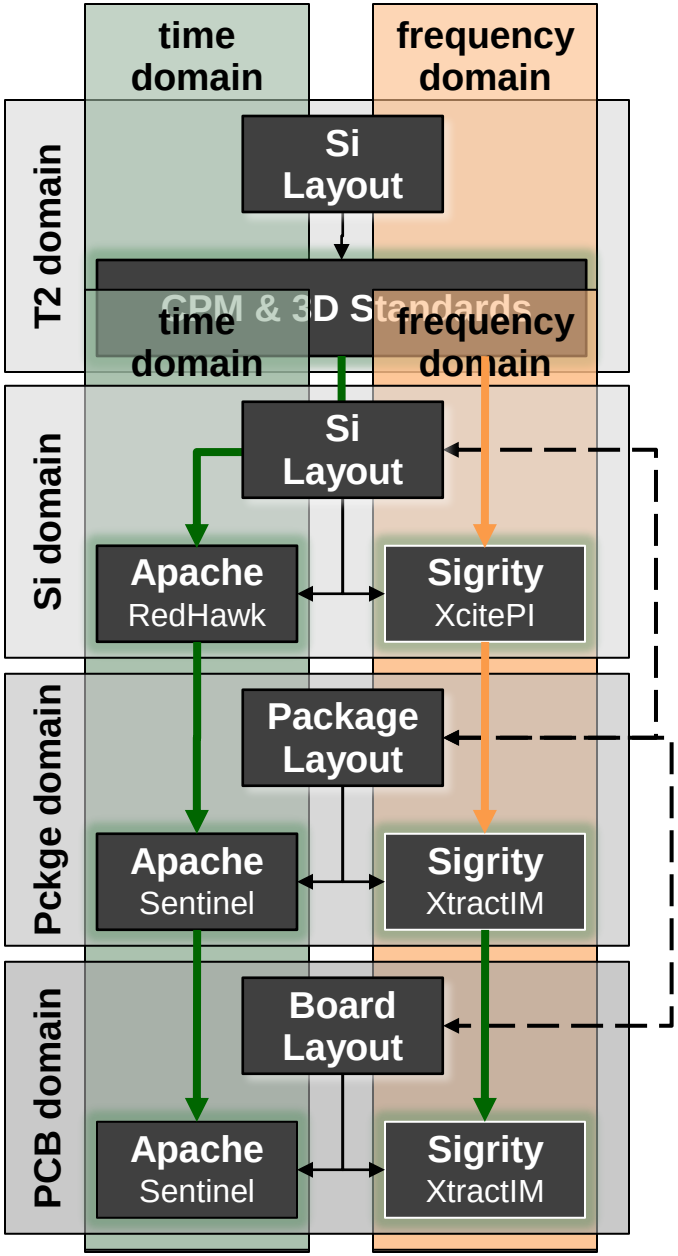
- Next : Integrated Stack Designs
 - e.g. Logic-on-Logic or Interposers
 - Design Methodology Requirements
 - Integrated PD Co-Design w Interposer & Substrate
 - Design Constraint Methodology
 - Design Authoring – including the Package
 - Manufacturability (aka TechTuning)



Evolving from 2D Design

3D PDN Design Flow

- 2D Ref Flow
 - Sign off in time domain (Apache)
 - Analyses in frequency domain (Sigrity)
- 3D PDN Flow Approach
 - ✓ Take as much as possible from ref flow
 - ✓ Similar approach as Si-Package-PCB Analyses
 - – Extract each tier separately
 - – Model as an integrated stack
 - ✓ Upgraded tools to understand new features
 - – TSV, uBump, BRDL, Tier n …
- Current Status
 - Demonstrated Tools & Flow
 - Supporting development of standard Compact PDN Models and associated 3D Design Exchange Format Standards



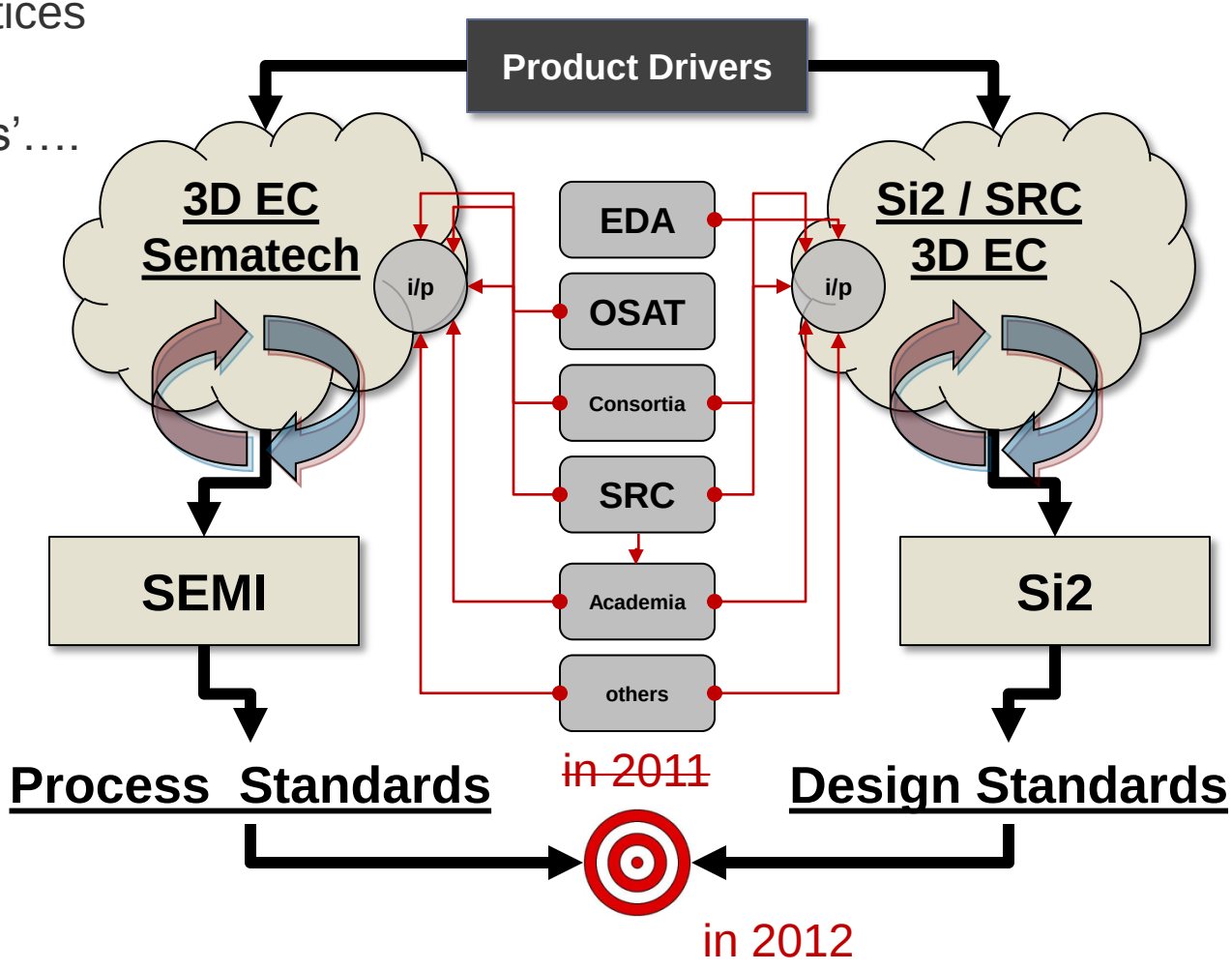
Inventory of Current Core Design Technologies

	PathFinding	TechTuning	Design Authoring
Things We Do Have	✓ 3D Floorplanner ✓ 3D Net generator ✓ PDN resource estimator	✓Package Stress simulator ✓Feature Stress simulator ✓Reference Thermal sim.	✓2D design flow & tools ✓Timing with a fixed TSV/uBump layout ✓ 3D aware PI / SI analyses
Things We are Working On	• Package PathFinder • System PathFinder • Standard 3D design exchange formats	• Chip Level Stress Sim • Chip thermal floorplanner • Standard 3D design exchange format & PDK	• M-o-L product design • 3D Variability Flow • Standard 3D design exchange formats
Things we do NOT Have (and wish we did)	Technology PathFinder	3D in flow substrate coupling analyse Fully supported TechTuning "PDK' System component thermal co-design	TBD Logic on Logic TBD Interposer TBD 3D Extraction TBD 3D ++ (see below)

- We don't have Everything – but we do have much more than Nothing ☺ !!

Standards : a Lubricant for the Supply Chain

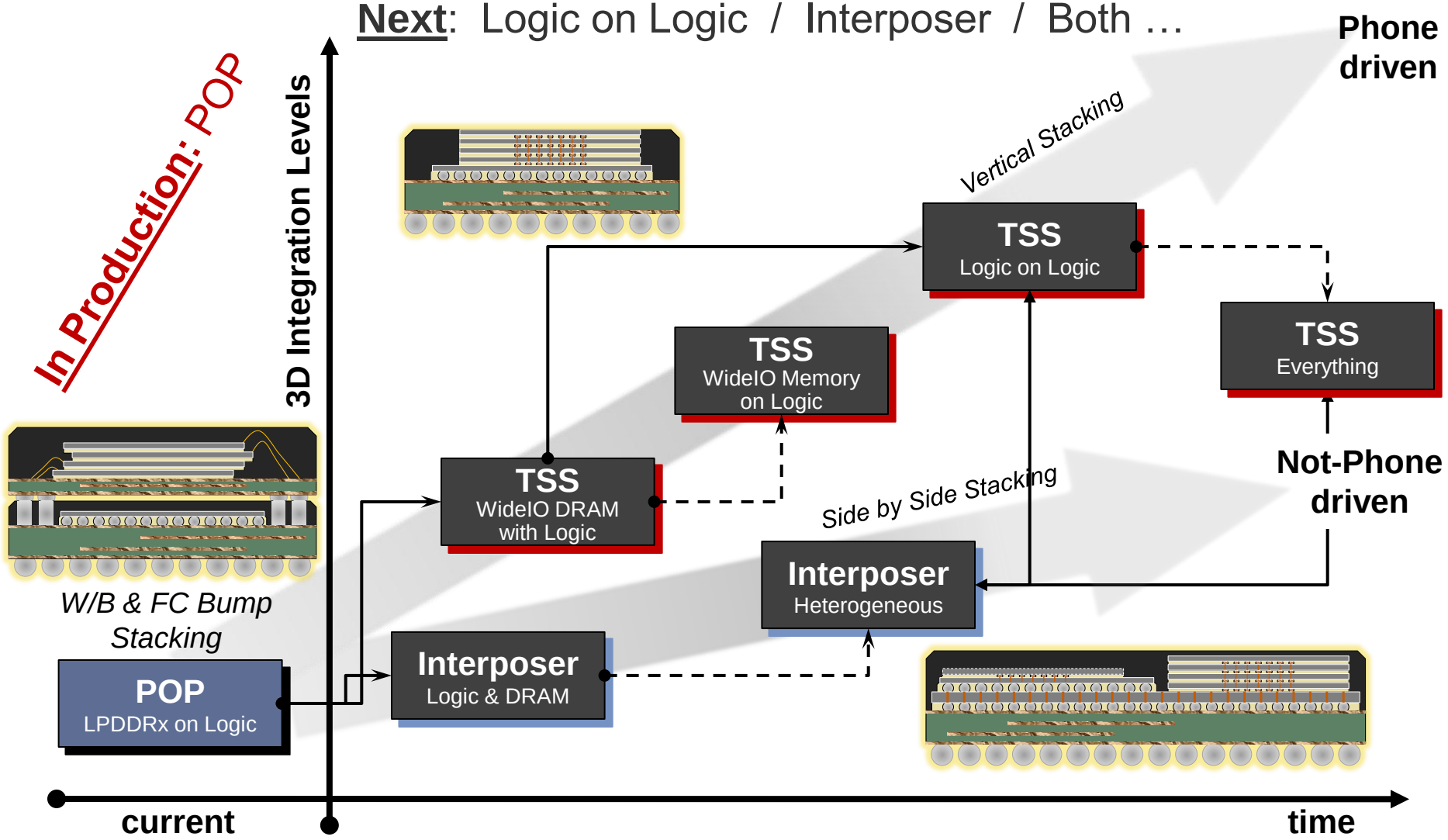
- **Leverage Existing Standards Bodies**
 - Established balloting, adoption and management practices
 - But formal and hence need ‘mature proposals’….
- **Process Standards**
 - 3D Enablement Center
 - Sematech
 - SEMI …
- **Design Standards**
 - Si2
 - 3D EC / SRC
 - IEEE
 - JEDEC…
- **Encourage Participation by the Industry – esp EDA**



2.5D / 3D Stacking Roadmap

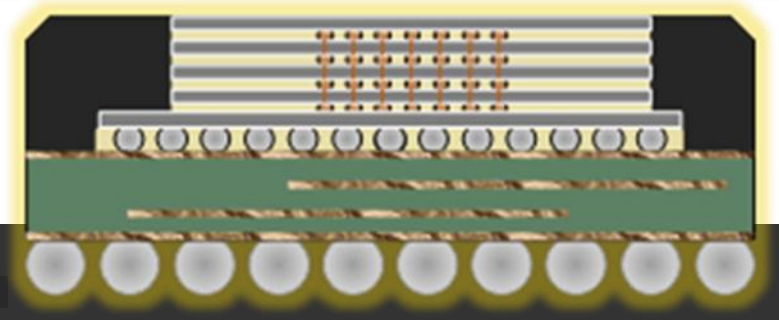
Our Current Focus: Wide IO DRAM on Logic = TSS

Next: Logic on Logic / Interposer / Both …



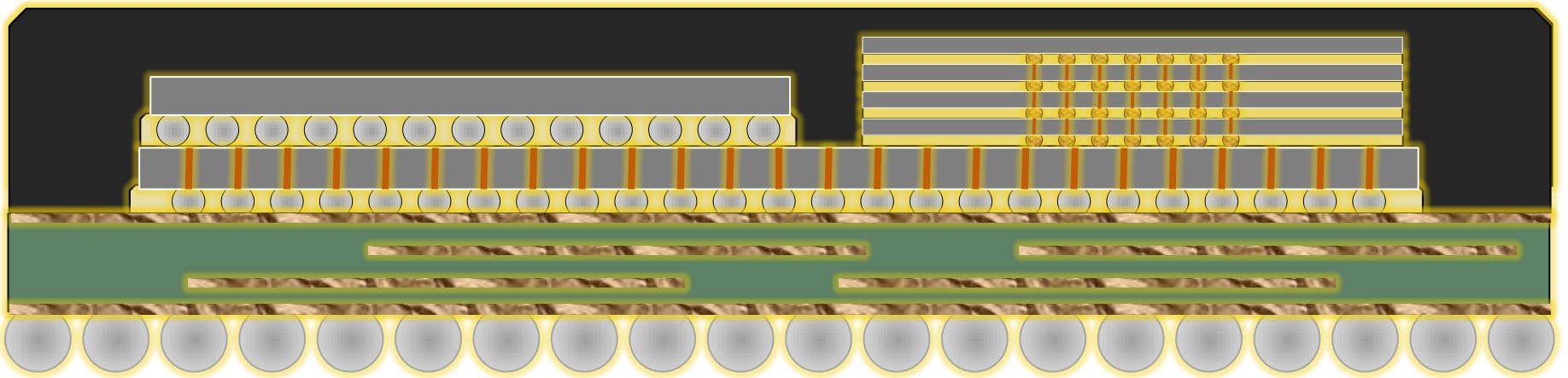
Design Environment for Memory-on-Logic

Status	Arena	Item
Have	**Design**	✓ 2D design flow & tools + quasi-manual placement of T2T / TSV array + custom T2T buffer design & incremental rules to manage interactions
	Timing	✓ 2.5D analyses flow & tools + compound 'lumped' TSV delay model
	PI	✓ 2D analyses flow and tools + extended hierarchy + recognition of new features
	SI & Variability	✓ 'Off Line' analyses to produce set of 'keep out' rules
In Flight	**'In Line' Rule Checkers**	✓ Chip Level Stress Simulator – for 'stress Hot Spots' ✓ Chip Level Thermal Floorplanner ✓ Chip Level SI Simulator
	Integration w/ Commercial Die	✓3D Design Exchange Formats
Like to Have	**SI Analyses**	In Flow SI analyses – on line and in product flow
	TechTuning & PathFinding	Fully supported TechTuning "PDK' System-Component thermal co-design



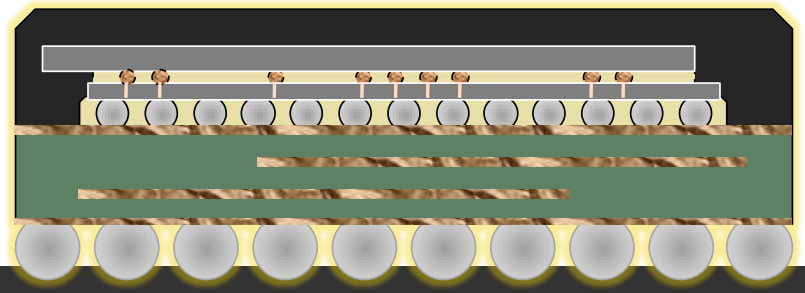
Design Environment for Interposers

Status	Arena	Item
Have	Design	✓ 2D Layout tools ✓ 2D Extraction Tools
Need to Have	Extraction	Integrated 3D Extraction inc. TSV , routing and FRDL/BRDL
	Signal Integrity	Integrated SI tools inc floating substrate and 3D features
	Power Integrity	Integrated PI analyses tools & flow
	DFT / Test	Integrated Double Sided Passive Floating Substrate
	PathFinding	Architectural Trade Off Analyses for Value Proposition

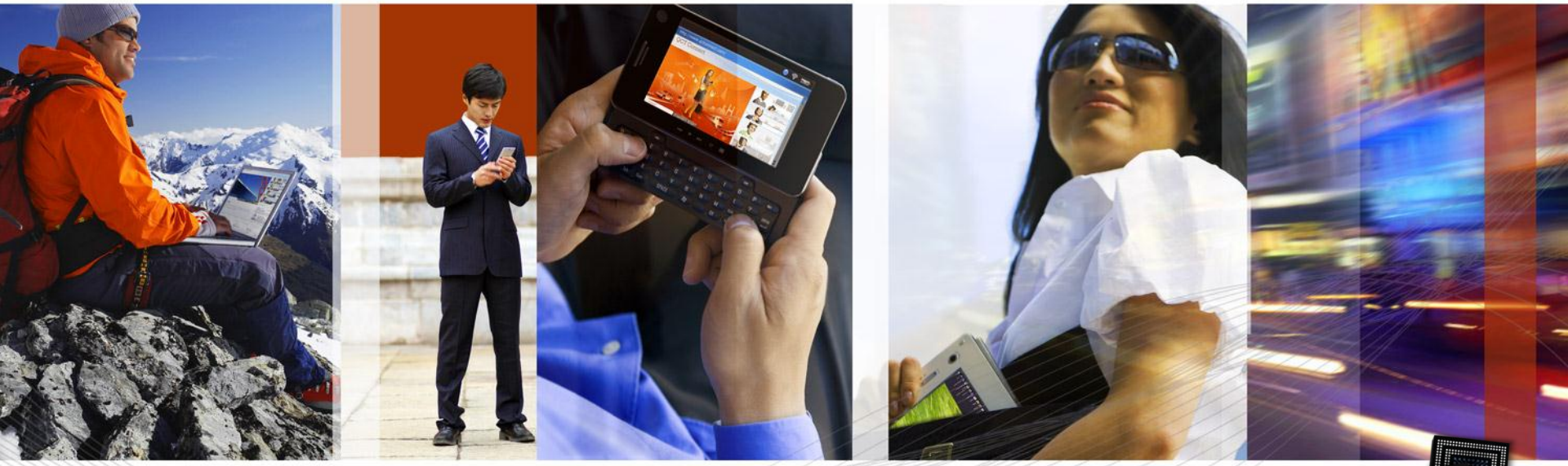


Design Environment for Logic on Logic

Status	Arena	Item
Have	Design	✓ 2D Flow for One Single Sided Die & Technology at a time
	PathFinding	✓ 3D Physical PathFinding Flow for finding Value Propostion
Must Have	Floorplan	3D with optimization across multiple tiers (technologies)
	Utility Insertion	3D tools for global utilities – eg NoC, Clock, DFT….
	Extraction	3D Extraction inc. TSV , routing and FRDL/BRDL
	Timing	across multiple tiers, technologies, libraries….
	Power Integrity	Integrated PI analyses tools & flow
	Signal Integrity	in flow SI analyses tools inc 3D features
	DFT / Test	Optimized DFT overhead for pre-stack test
	Verification	3D Physical Verification, LVS, etc across multiple tiers
	etc..	dependent on the actual stack partition



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QUALCOMM® CDMA Technologies

REDEFINING MOBILITY

THANK YOU



Xilinx SSI Technology
Concept to Silicon Development Overview

Shankar Lakka

Aug 27th, 2012

Agenda

- Economic Drivers and Technical Challenges
- Xilinx SSI Technology, Power, Performance
- SSI Development Overview
- Summary

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Market Dynamics

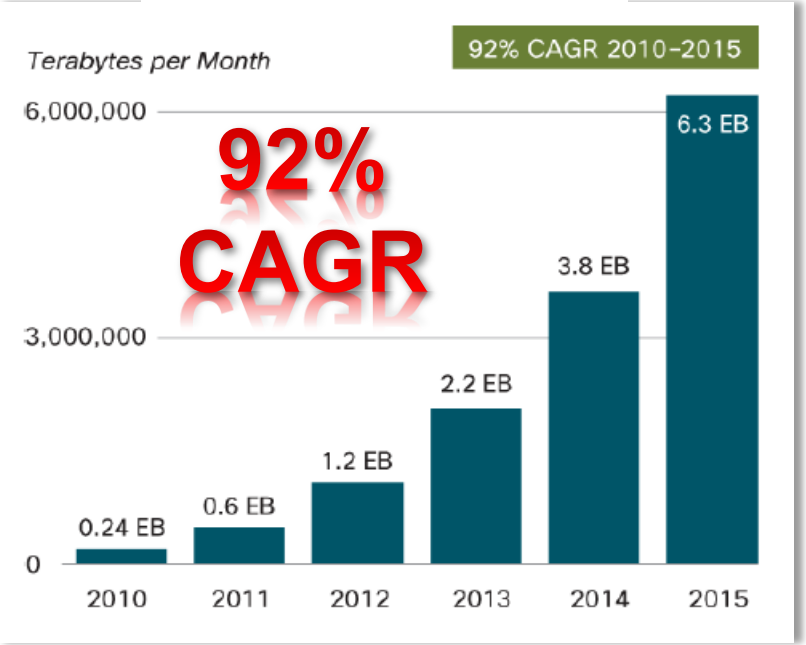
Video Driving Explosive Growth in Traffic

By 2015 2/3 of Mobile Traffic will be Video

Machine to Machine

- **Smart Meters, Security Cameras, Health Care, Telematics, etc.**

Mobile Data Traffic



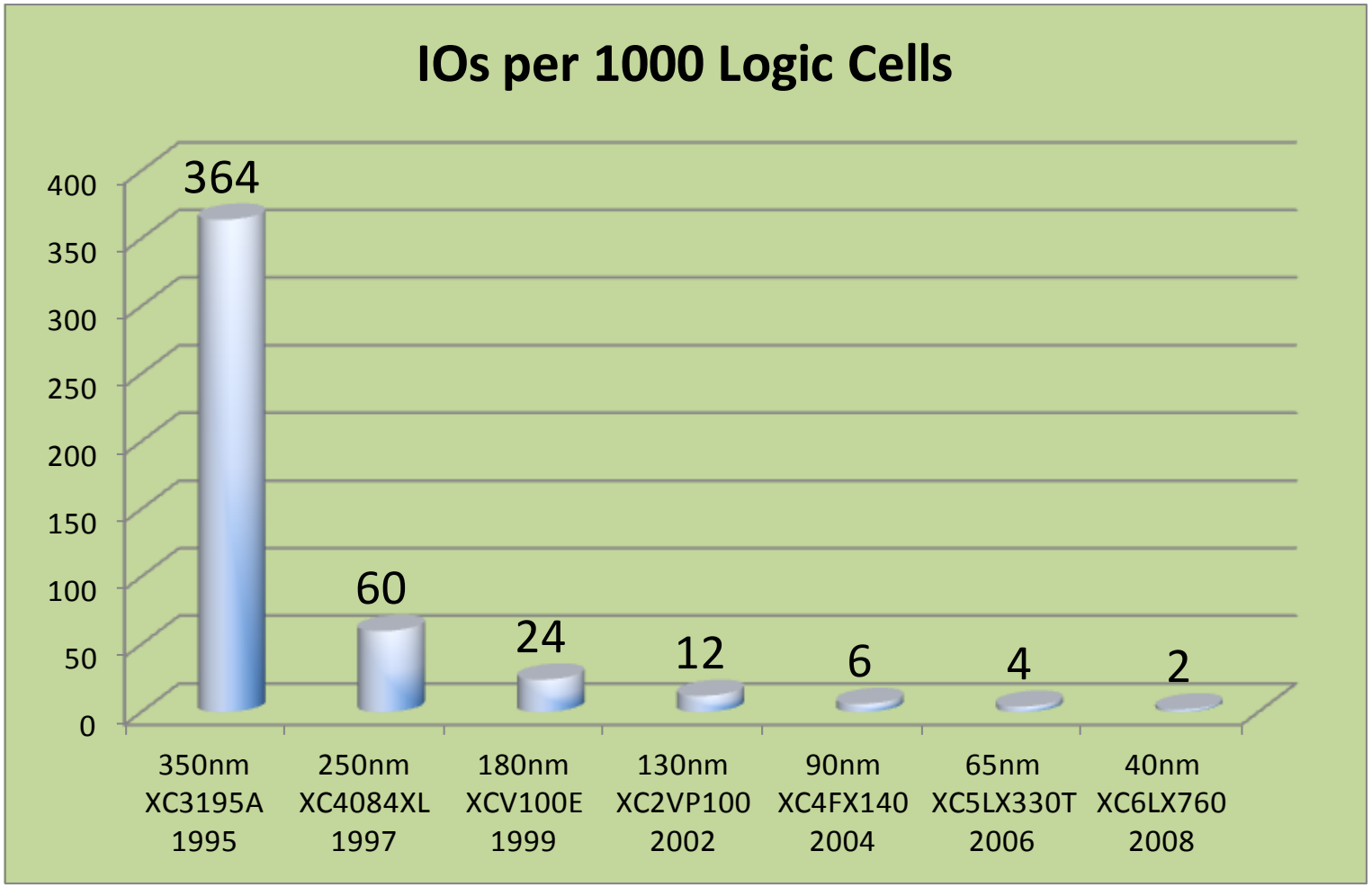
2x Bandwidth growth every 3 years at the SAME POWER BUDGET

Source: Cisco Global Mobile Traffic, January 2011

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On Die IOs Not Scaling

Number of I/Os per 1000 logic cells in the largest FPGA in each family

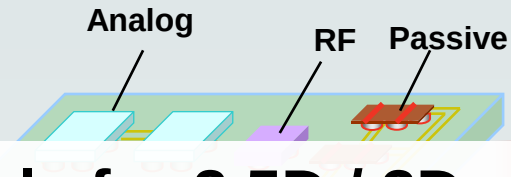


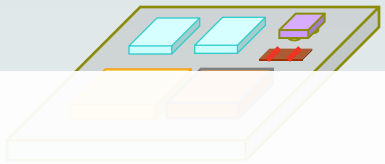
Logic doubles with Moore's Law but I/O quantity does not

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The Progression of 3D Technology

Traditional MCM/PCB	Silicon Interposer 2.5D	Full 3D







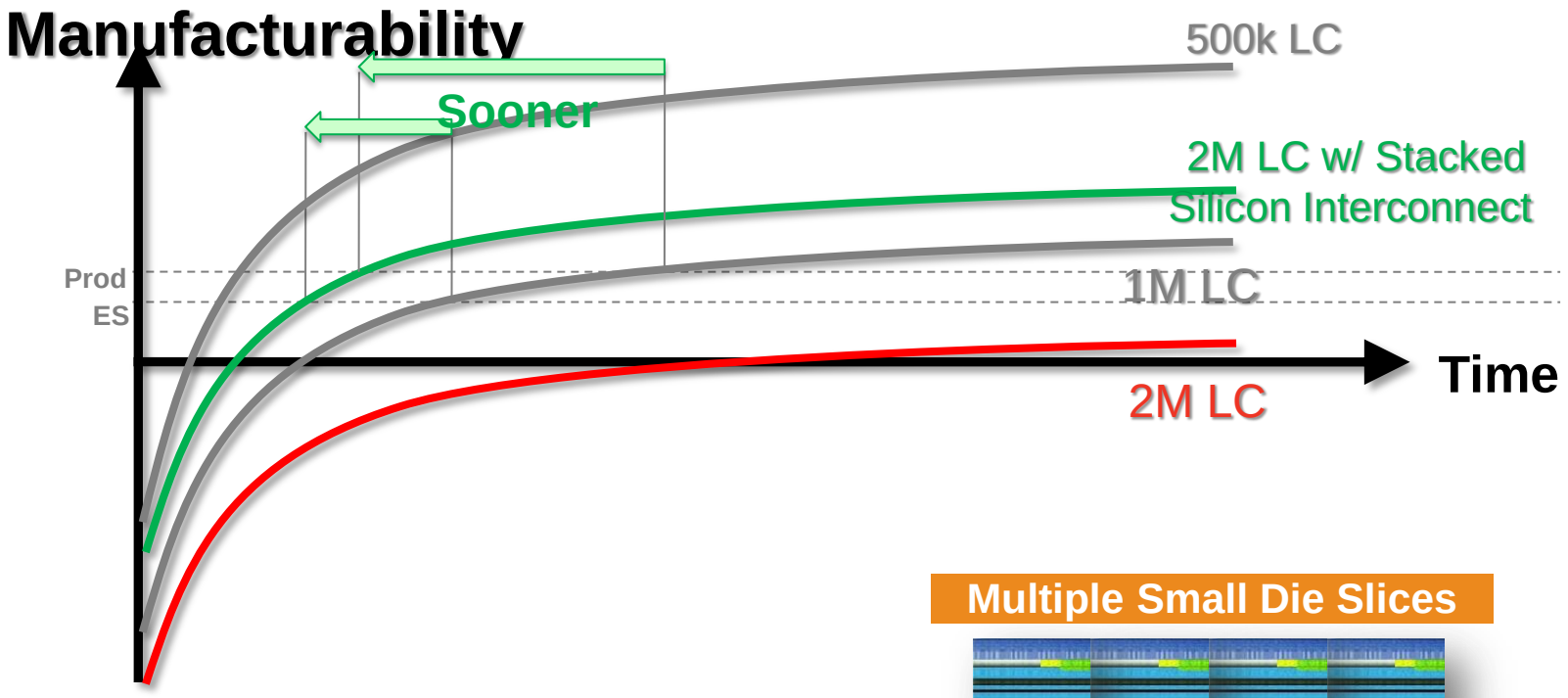
Goals for 2.5D / 3D

- Connectivity: Break die to die IO bottleneck
- Capacity: Achieve Integration beyond Moore's Law
- Power: Reduce Total Power
- Heterogeneous SOC's: Mixed Functions & Processes

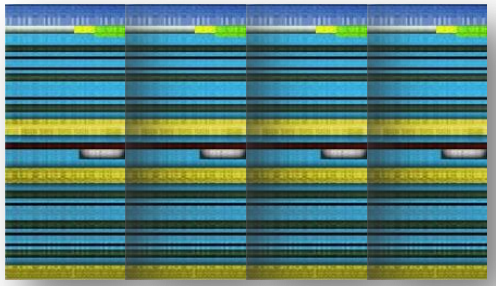
Source: TSMC

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Capacity : Beyond Moore's Law



Multiple Small Die Slices

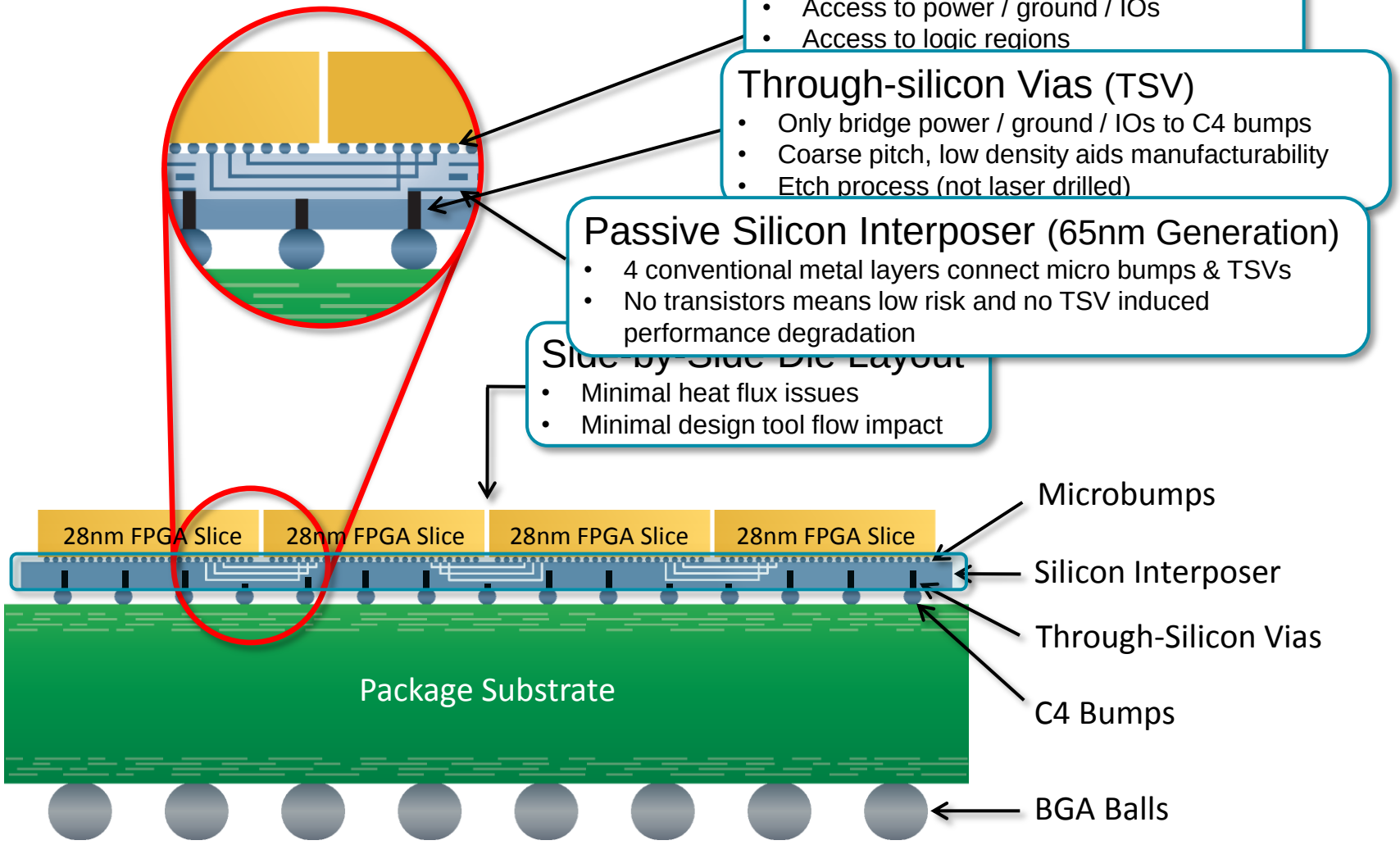


✓ **Greater capacity, faster yield ramp**

Reference:
Node N to N+1 ~ 1.5 to 2 years for Xilinx FPGAs

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Well published technology boiler plate

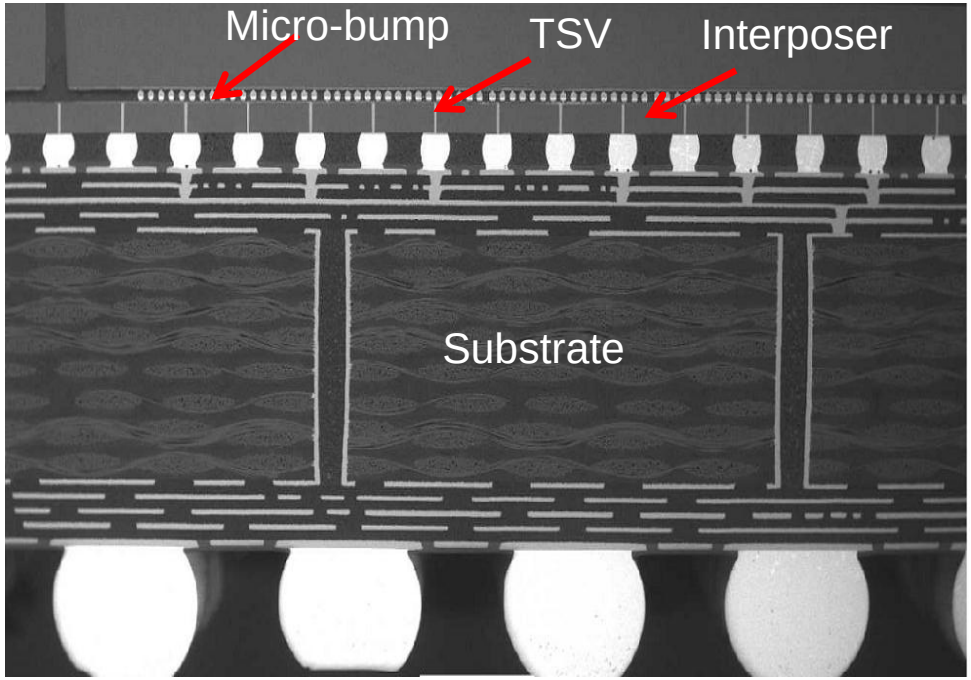


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Cross-section of 28nm FPGA with SSI

Virtex-7 2000T

28nm Active Die + 65 nm Passive Interposer



Courtesy of Xilinx, TSMC, Amkor

Interposer /Package Technology

Technology	Specs
M1-M4	2um pitch 4 4X layers
TSV	12um diameter & 180um pitch
Micro-bump	45um pitch
C4	180um pitch
Package	6-2-6 Layer, 1.0 mm BGA pitch

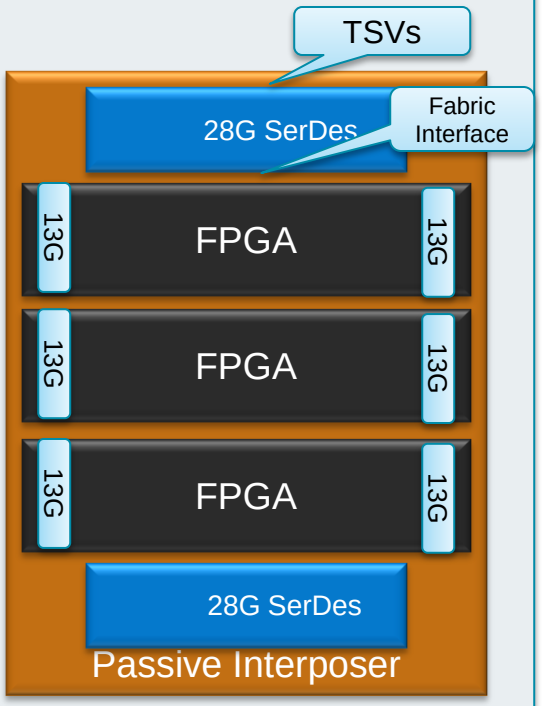
- Low risk approach to integrate TSV & u-bump
- High density micro-bump for ~50K chip-to-chip connections
- Better FPGA low-k stress management with silicon interposer

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Heterogeneous FPGAs with SSI

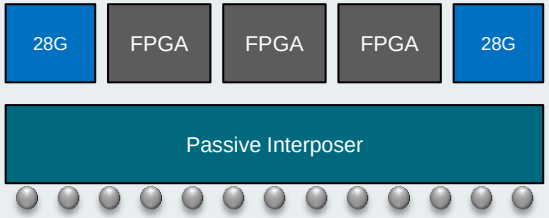
Virtex-7 HT

Top View



- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 IO

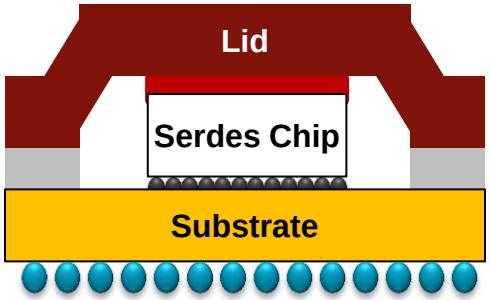
Cross Section

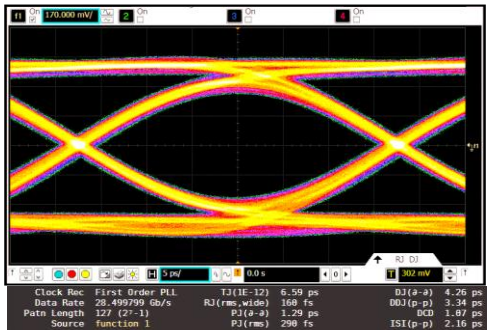


- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

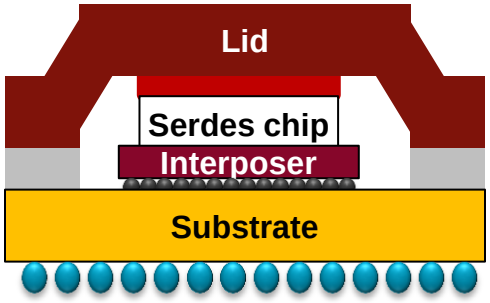
© Copyright 2012 Xilinx Inc.

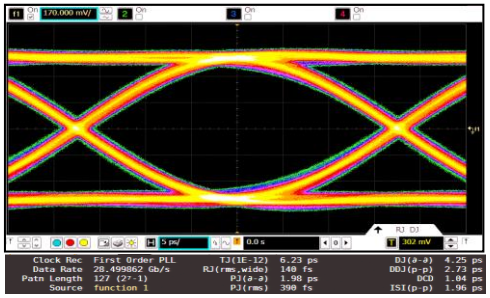
2.5D Performance vs. Monolithic





Vehicle 1 - Monolithic packaged 28Gbps Serdes





Vehicle 2 - 2.5D packaged 28Gbps Serdes

- **Measurements show 2.5D comparable performance to Monolithic die**

- Diagrams not drawn to scale

Reduced noise and better performance margin with SSI

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2.5D / SSI Takeaways

- **SSI Technology summary**
 - Capacity beyond Moore's law, Faster yield curve
 - Breaks die to die IO bottleneck
 - Heterogeneous SOCs
 - Power advantage

 - Stepping stone to true 3D

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SSI Implementation Overview



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Challenges for 3D design and validation

- **What areas of design validation and sign off are challenging for 3D and why?**
 - Circuit Design and Schematic capture
 - RTL, Physical Design of Top Die and Interposer
 - Extraction
 - Functional and Physical Verification (LVS, DRC)
 - Chip level functional verification
 - STA
 - IR/EM/SI or other Electrical analysis
 - Assembly and Yield (beyond the scope of this presentation)

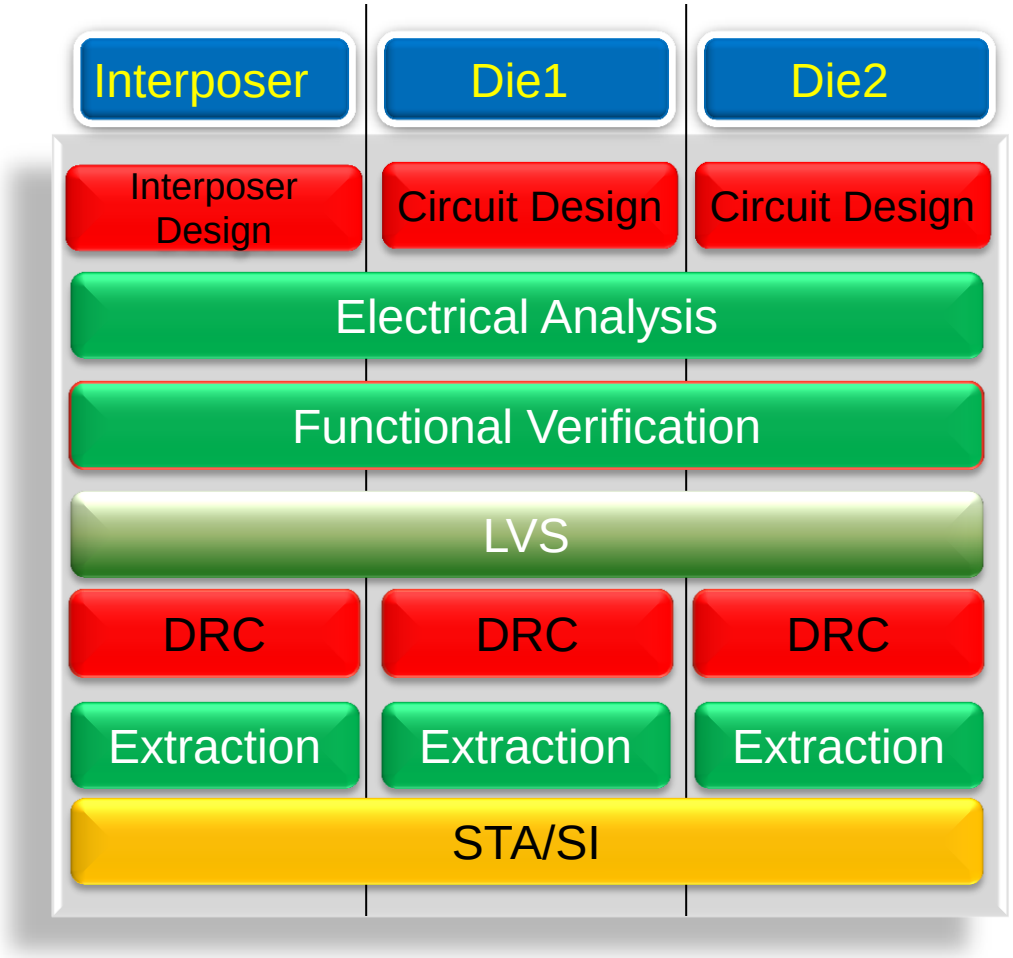
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Analysis and Sign off

State of EDA tools

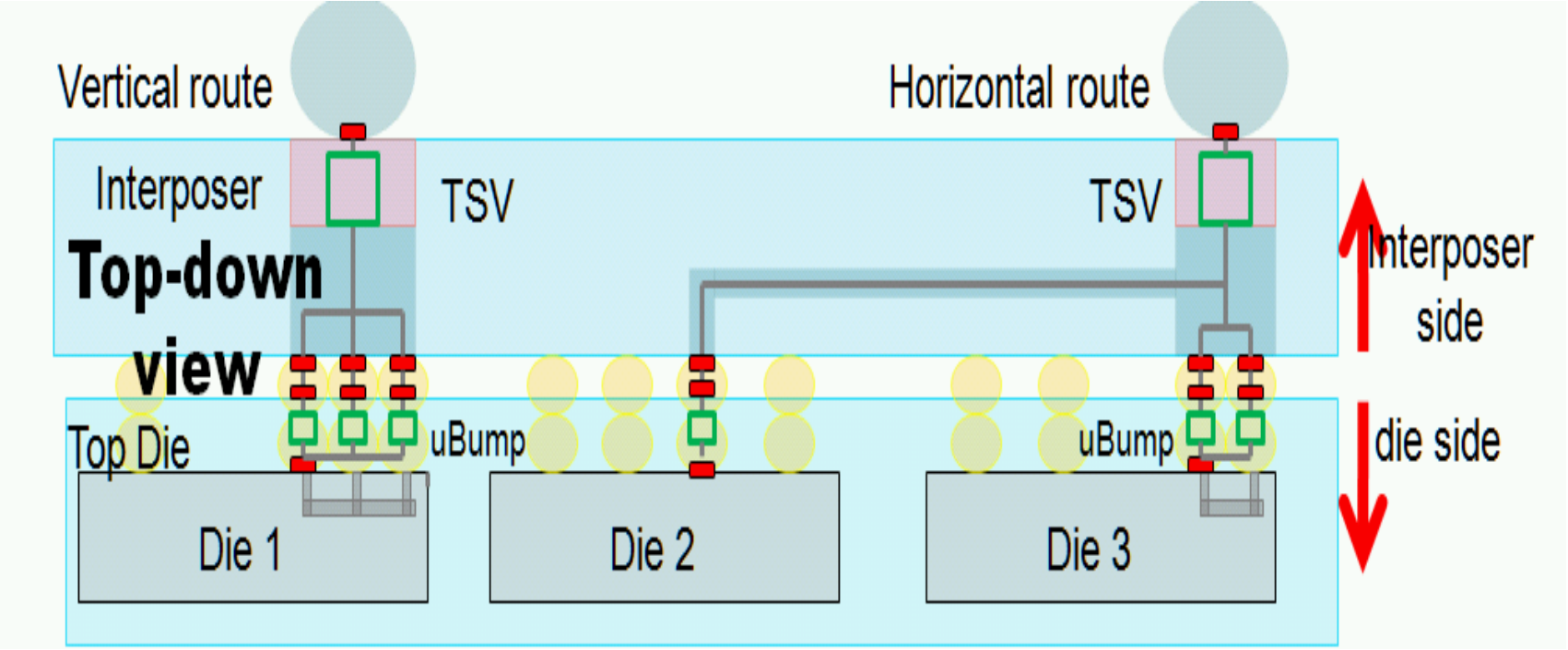
1. Can the analysis be split into hierarchical independent levels?

2. Can the data for analysis be split into hierarchical independent levels



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SSI Full chip



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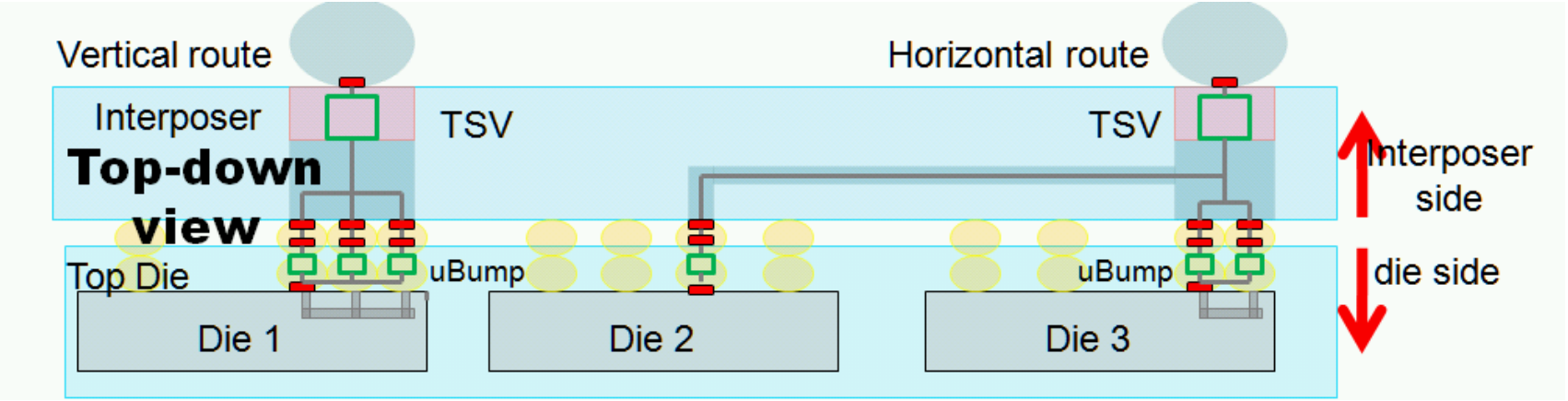
Circuit and Physical Design

- **Circuit Design and Schematic capture**
 - Electrical modeling of Interposer
 - Design of driver and receiver
 - HSPICE Simulations with process models from multiple process nodes
 - Signal Integrity analysis
 - ESD considerations
- **Physical Design, Extraction and Verification**
 - Manual vs. Auto-routed Interposer
 - Like Top Die (e.g. all FPGAs) vs. unlike Top die (FPGAs, w/ 28G SerDes)
 - Extraction of Interposer layout
 - LVS done on each Top die and multiple die together;
 - DRC done on Interposer and Top Die separately

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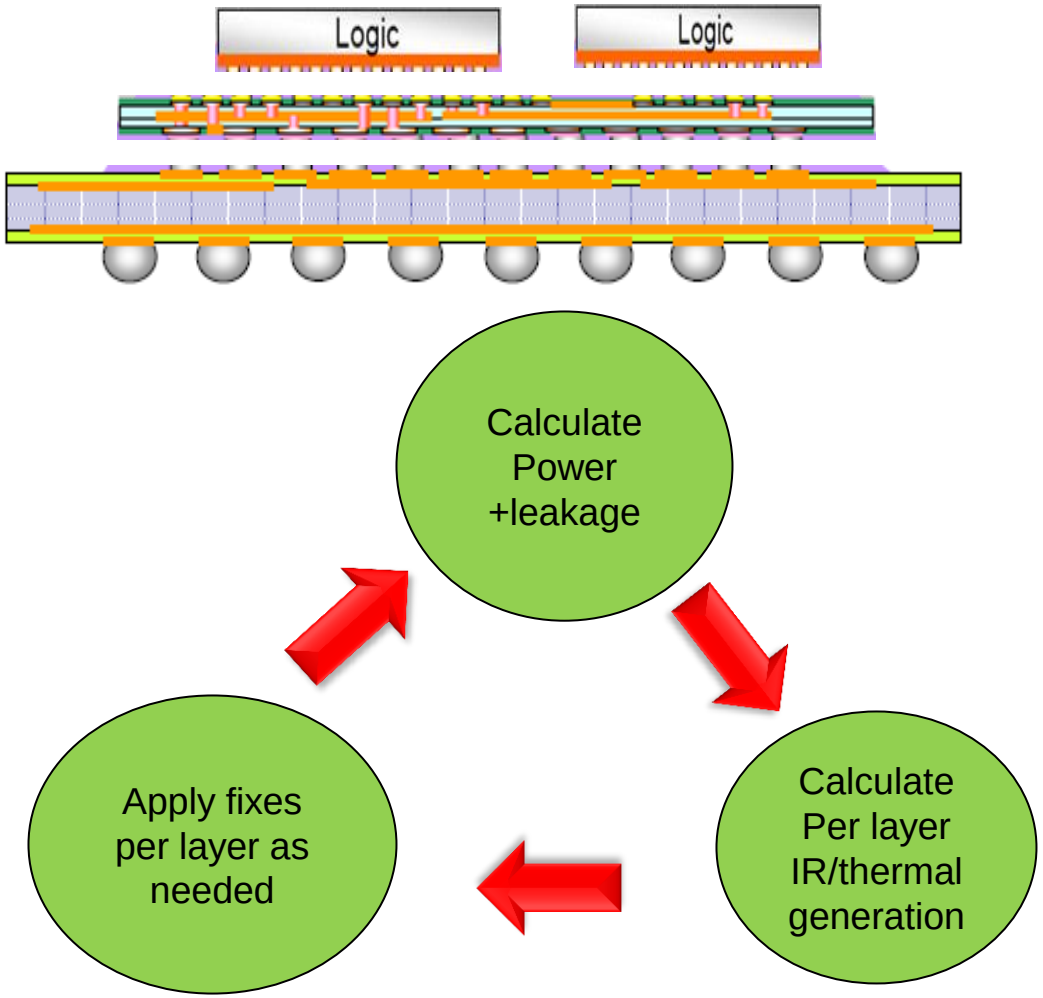
Static Timing Analysis

- STA
 - Black box ILM generated for each die
 - Full chip netlist (w/ extracted Interposer) generated using internal scripts
 - Special consideration given to the process distribution



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EM/IR and Thermal Analysis: Challenges



EM/IR by budgeting

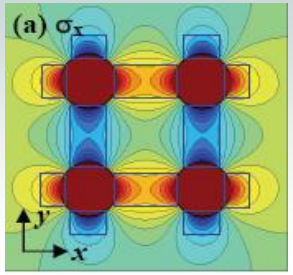
Accurate EM/IR and thermal analysis is iterative in stacked Die Scenario.

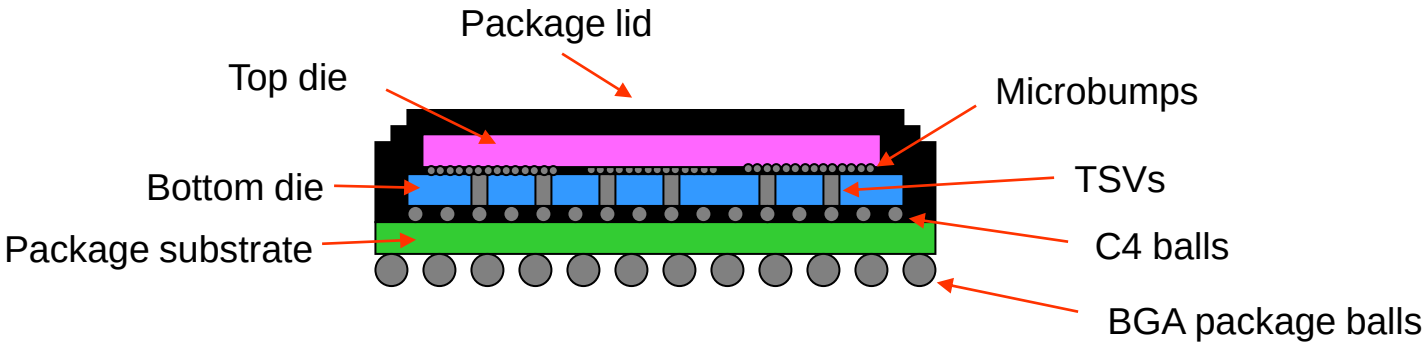
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3D: The next frontier

- **Higher performance chip stacked on top**
 - Thermal considerations
- **Bottom die includes power TSV's for top die**
 - Can be in older, "TSV-friendly" technology
- **Floor-planning is critical:**
 - Thermal concerns (stacked thermal flux)
 - TSV keep out zones may be required in bottom die to avoid stress-induced performance impact

TSV-Induced Device Stress





Assembly Technology still evolving

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Call-to-Action: Develop & Evolve 3D Standards

- **Design enablement**
 - Interposer Models
 - EDA Tools for 3D development and verification
 - Chip-to-chip interface standards
- **Manufacturing standards**
 - DFM rules for TSV, microbump
 - Materials: TSV, u-bump
 - Thermal budget
- **Test**
 - Test HW & u-bump probing
 - Known-Good-Die method
 - Self Test Required (FPGA programmability is an advantage)

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Conclusion

- **Bandwidth, power and cost demands are beginning to present significant challenges for monolithic silicon**
- **Stacked Silicon Interconnect is a breakthrough!**
 - Capacity
 - Connectivity
 - Power, Performance
 - Heterogeneous SOCs

SSI technology is the next big step in IC evolution

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Stacked Silicon Interconnect: A World of Difference



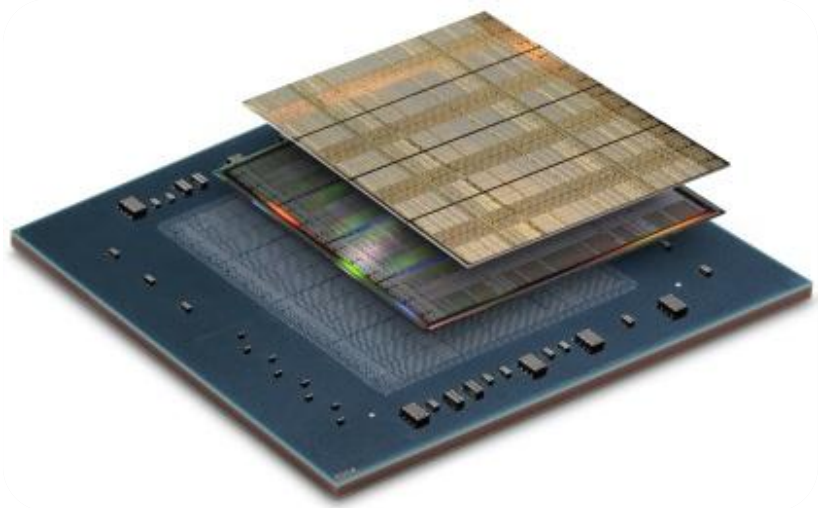
Earth

Area: ~500 Million km²

Population: ~6.8 Billion People

Oceans: 5

Age: 5 Billion Years



Virtex-7 2000T

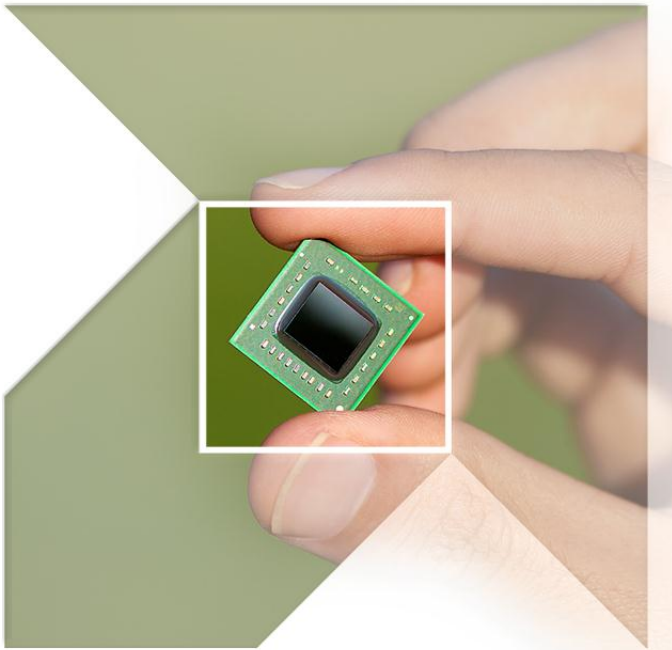
Interposer Area: ~775 mm²

Population: ~6.8 Billion Transistors

Chips: 5

Age: 40 weeks

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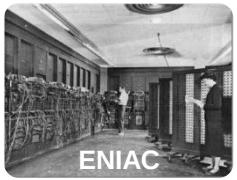


DIE STACKING AND THE SYSTEM

August 27th, 2012

AMD

SYSTEM TRENDS IN THE INDUSTRY



Source: Wikipedia



Source: uh.edu



Source: microsoft.com



Source: ibm.com



Source: laptopsarena.com



Source: applefriend.com

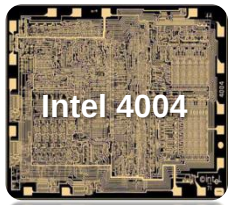
40’s | 60’s | 80’s | 90’s | Now

Increasing Performance Density

- The industry is driving performance density
- Improvements in performance density are driving new form factors
- New form factors discover new usage models
- Without new usage models the industry stagnates

MOORE'S LAW ENABLES SI INTEGRATION DRIVING NEW FORM FACTORS

µProcessor

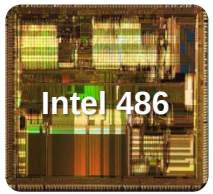


Source: proyectoyautja.proboards.com

1971

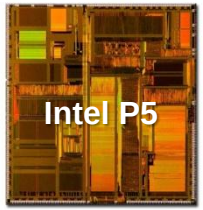
Cache & FPU

1989



Source: gecko54000.free.fr

Multi-Media

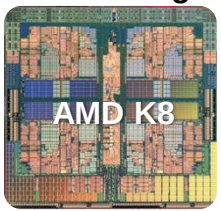


Source: gecko54000.free.fr

1993

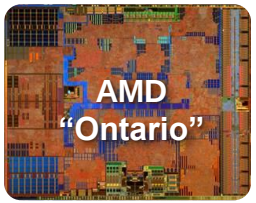
2003

North Bridge



Source: barcelona.com

Graphics



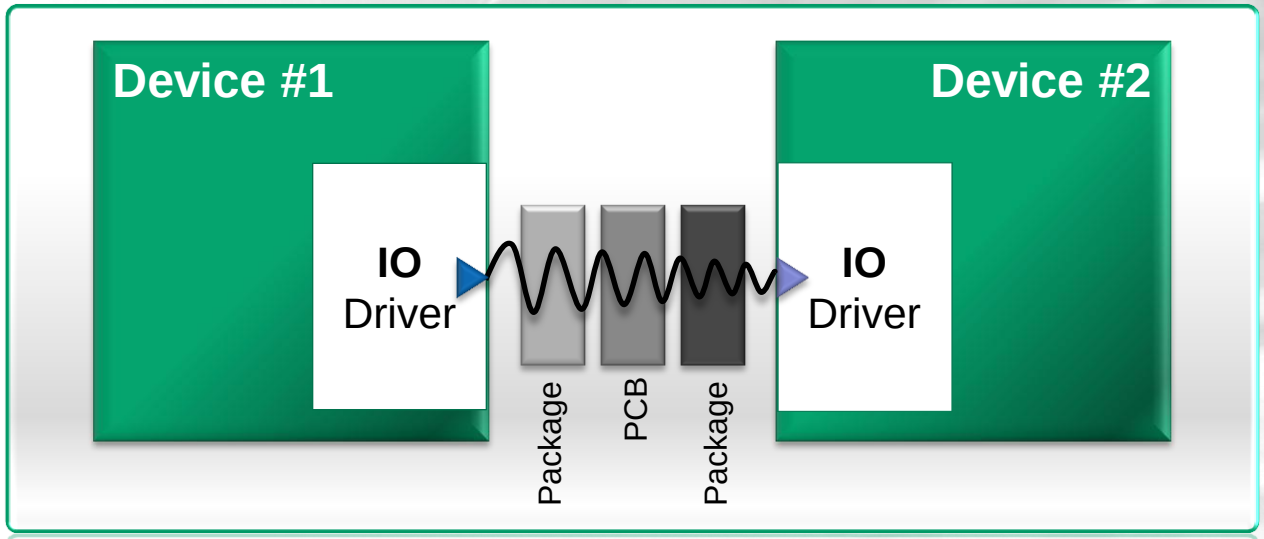
Source: AMD

2010

South Bridge is Next

THE OBVIOUS ADVANTAGE OF INTEGRATION

- Communication is overhead costing power, latency, and footprint

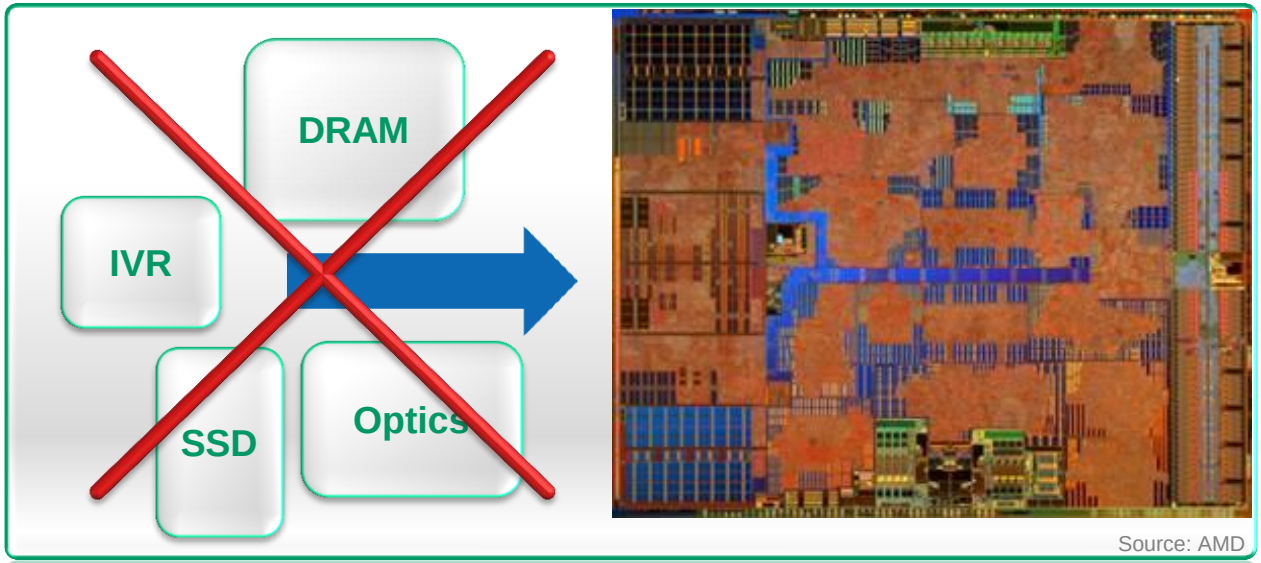


- Interface power is proportional to bandwidth and the link RCs
- And... BW is limited by the off die interface which doesn't scale fast
- But… off die BW demand increases with transistor density

AMD

SI INTEGRATION IS RUNNING OUT OF GAS!

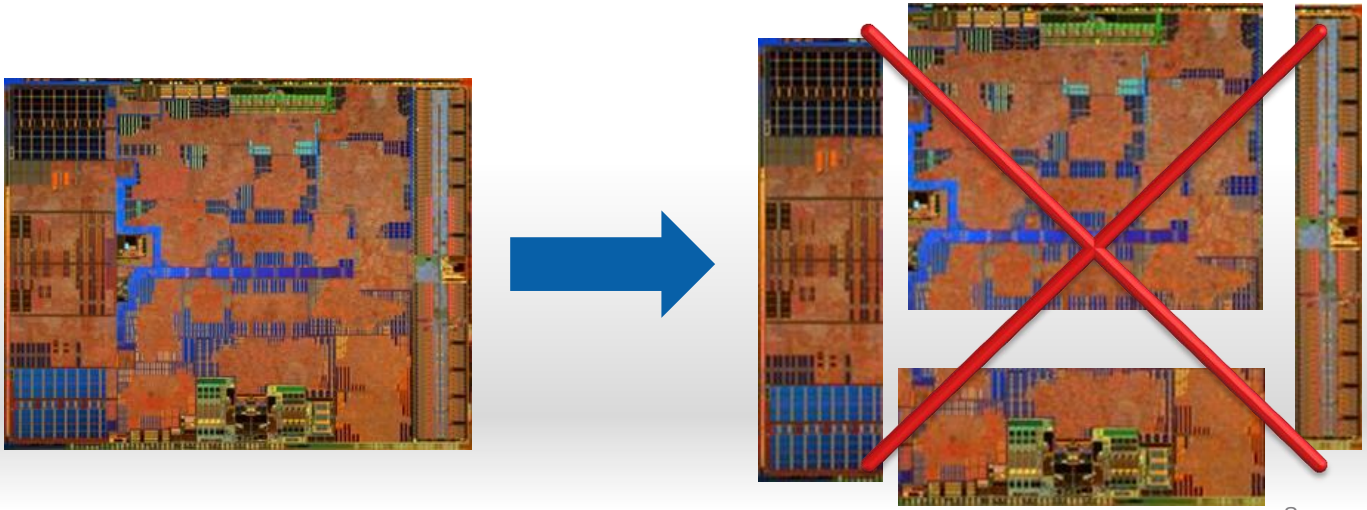
- Moore's Law will continue but there is a limitation
 - All similar technology components have been integrated such as Cache, FPU, Multi-Media, NB, GPU, SB, etc…
 - Only disparate technologies such as DRAM, SSD, IVR are left



Source: AMD

SI INTEGRATION IS RUNNING OUT OF GAS!

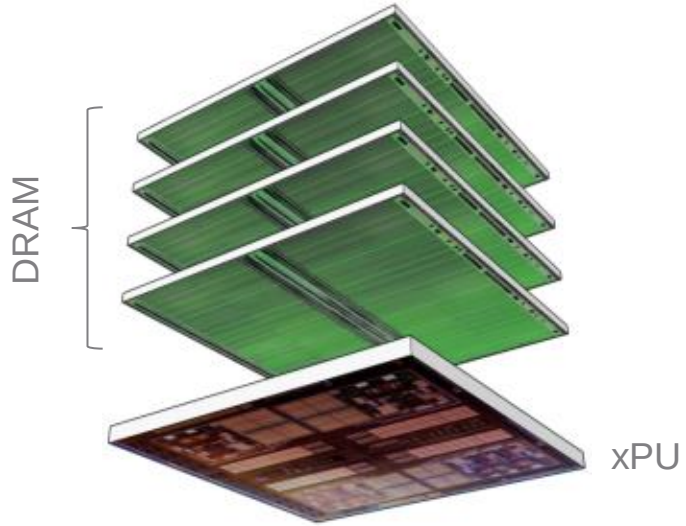
- Moore's Law will continue but there is a problem
 - Process scaling is going to stop supporting diverse functionalities on a single die such as fast logic, low power logic, analog, and cache
 - The single die will want to break into specialized components to maximize the value of new and existing process nodes



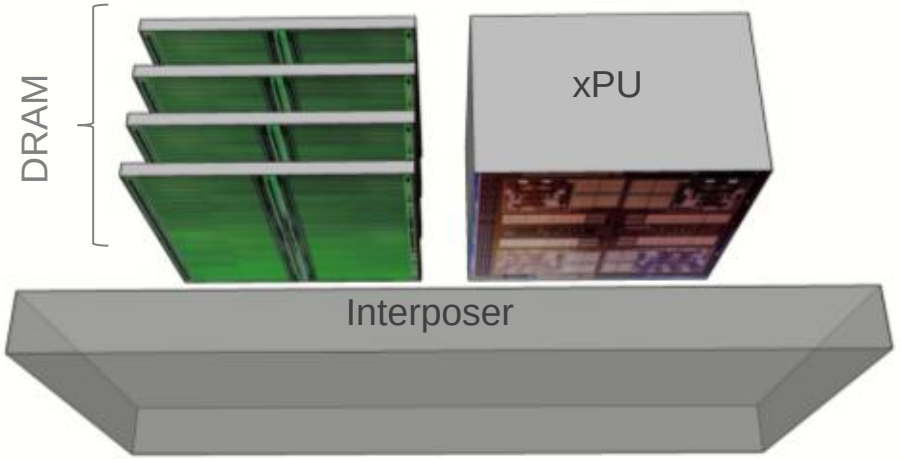
Source: AMD

TWO TYPES OF DIE STACKING

- Very similar technologies that reduce metal interconnect and improve proximity of disparate technologies allowing new levels of integration and process specialization

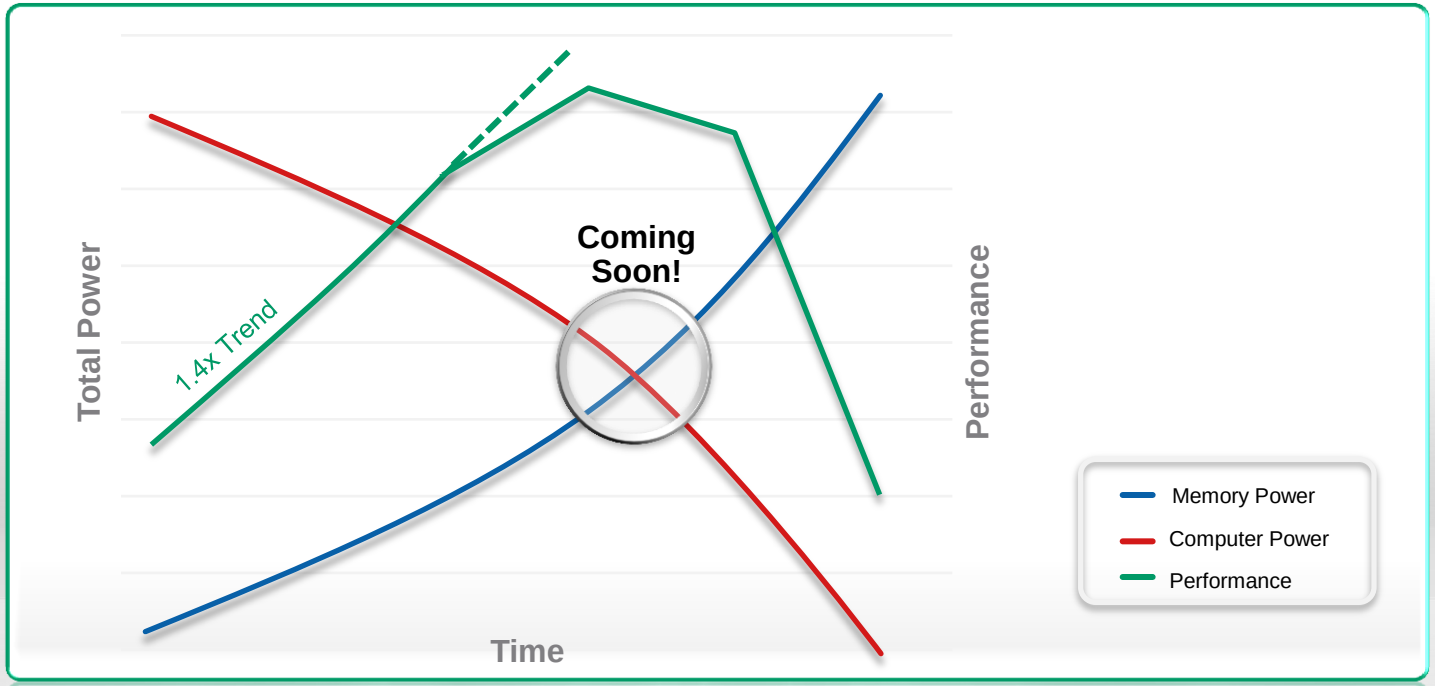


VERTICAL STACKING (3D)



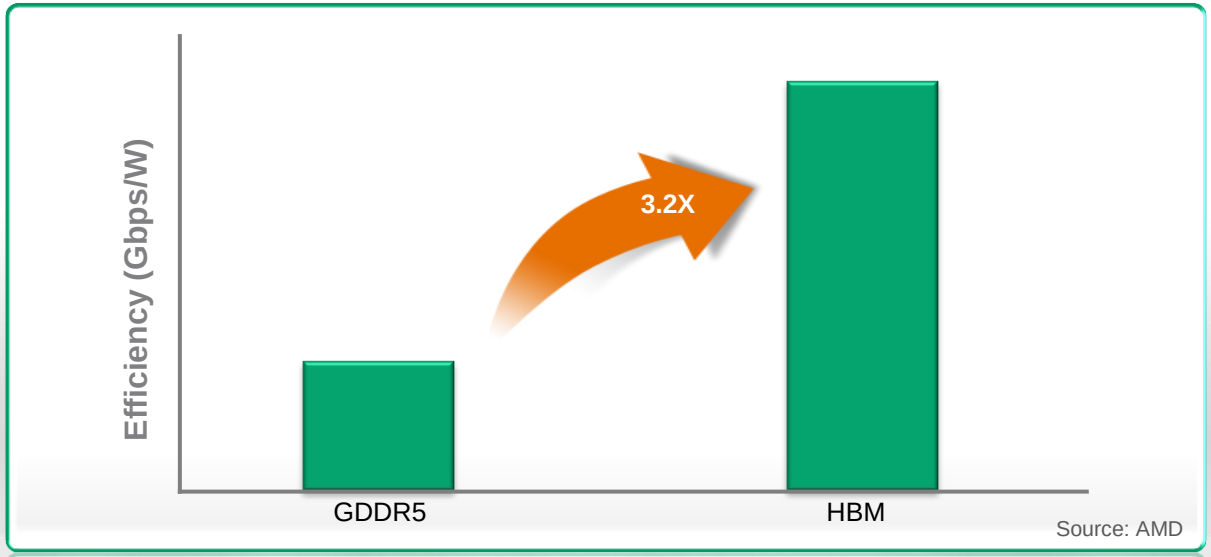
INTERPOSER STACKING (2.5D)

DIE STACKING MOTIVATION (MEMORY INTEGRATION)



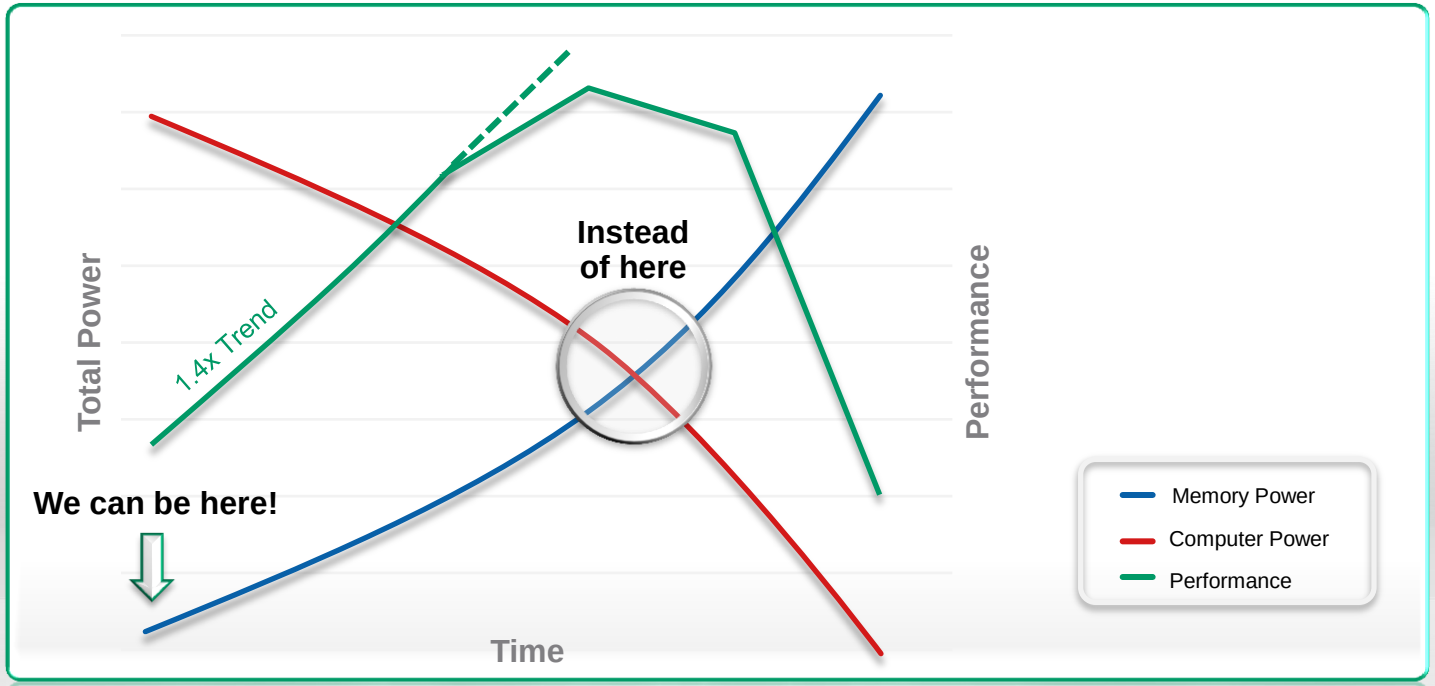
- System power is fixed in all platforms
- Compute performance in all platforms is proportional to memory BW
- Memory BW power increases with demand

IMPROVING BW/WATT WITH DIE STACKING



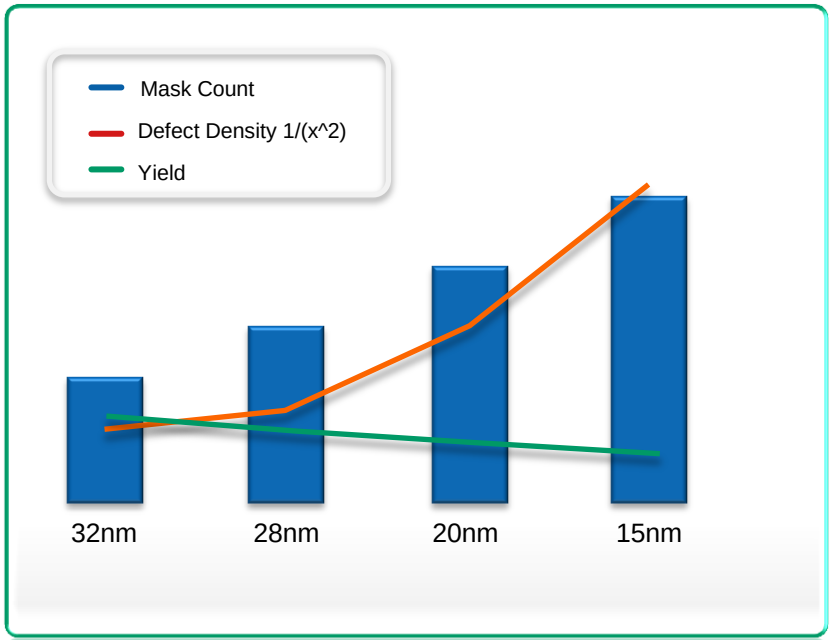
- Die stacking helps improve the proximity of the DRAM to Compute
- Dense and fine pitch interconnect enables simple low power interfaces as well as fine grain power control of the DRAM

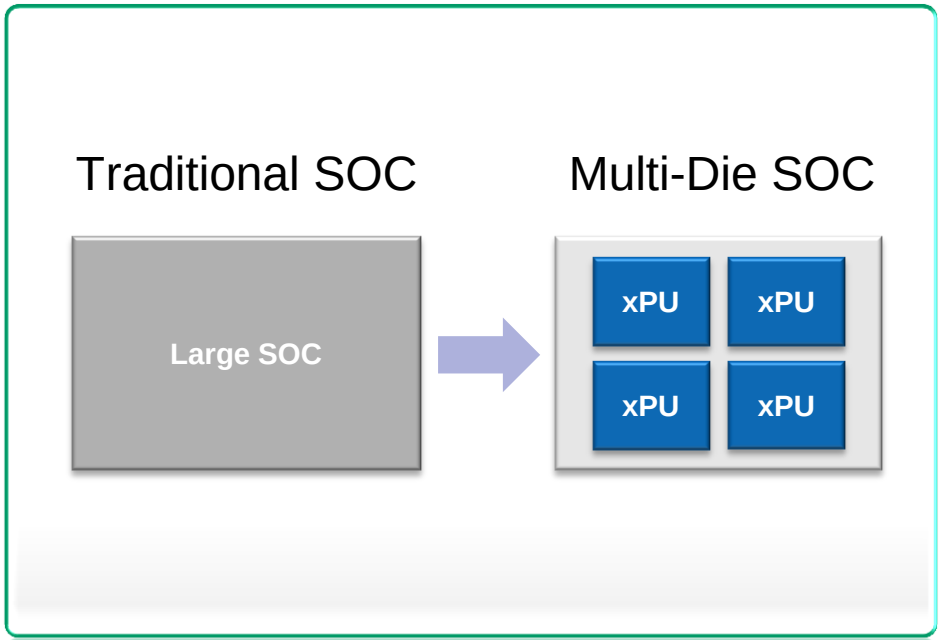
DIE STACKING MOTIVATION (MEMORY INTEGRATION)



- Dramatically improved memory BW/W rolls back the impact of recent memory system power growth and can help provide years of future scaling

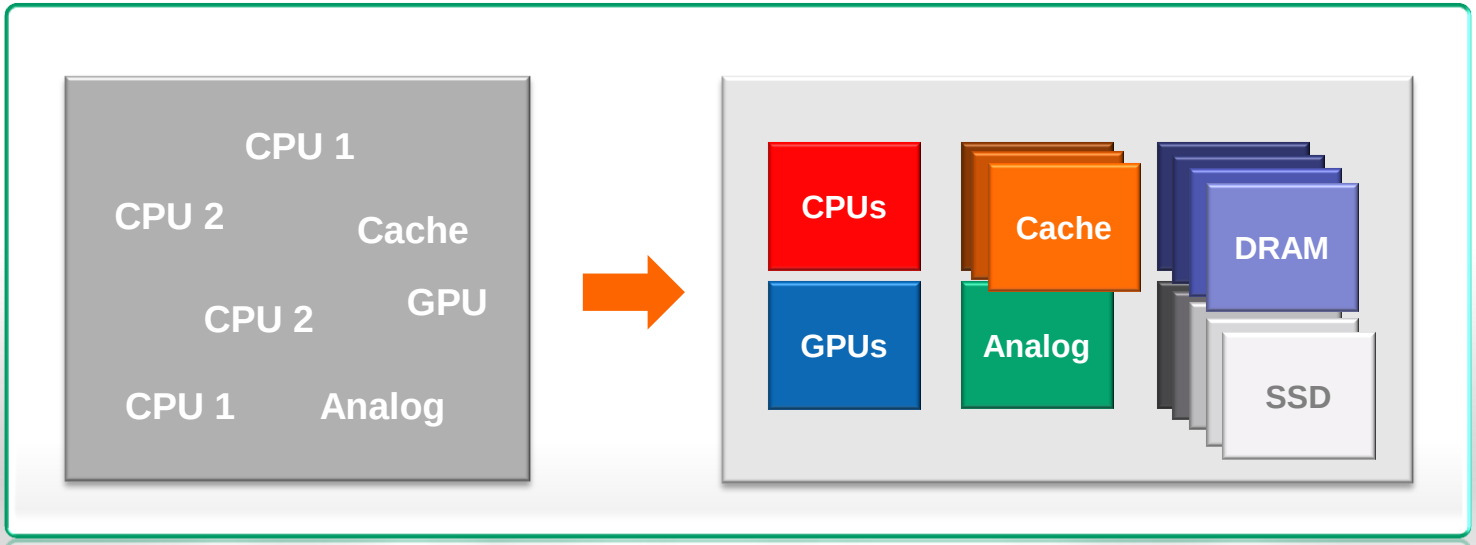
DIE STACKING MOTIVATION (LARGE DIE YIELD IS GETTING WORSE)





- Process complexity is increasing and yield is dropping as mask count increases
- Large die sizes will continue to have yield challenges

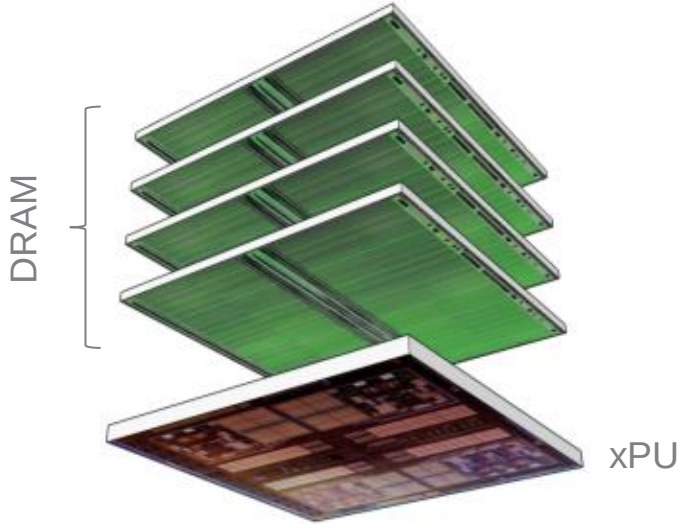
INTERPOSER WILL BE THE SOC WITH MULTIPLE 3D COMPONENTS



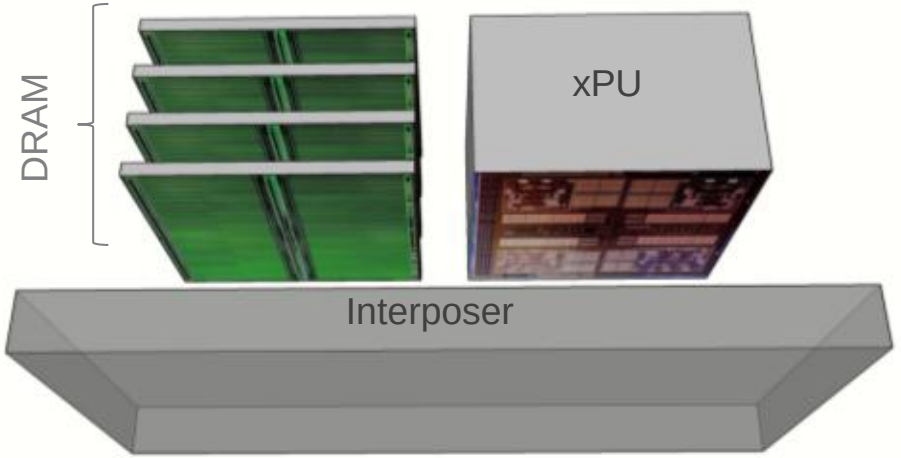
- Focus process node development on specific application functionalities
 - Reduce complexity and mask layer count
 - Reduce process node TTM
 - Reduce wafer runtime
 - Reduce wafer start cost
- Yield improves
- Functionalities scale at their own pace
- IP sharing includes test, reliability, and yield learning
- Improve performance, power, area, and cost of each functionality

AMD

CONCLUSION



VERTICAL STACKING (3D)



INTERPOSER STACKING (2.5D)

- Die stacking will enable new levels of system integration leading to new form factors and new usage models
- Die stacking will also help reduce process node complexity and improve yield and system cost

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Optical Backplanes with 3D Integrated Photonics?

Ephrem Wu
Sr. Director, Xilinx
Hot Chips 24, August 2012

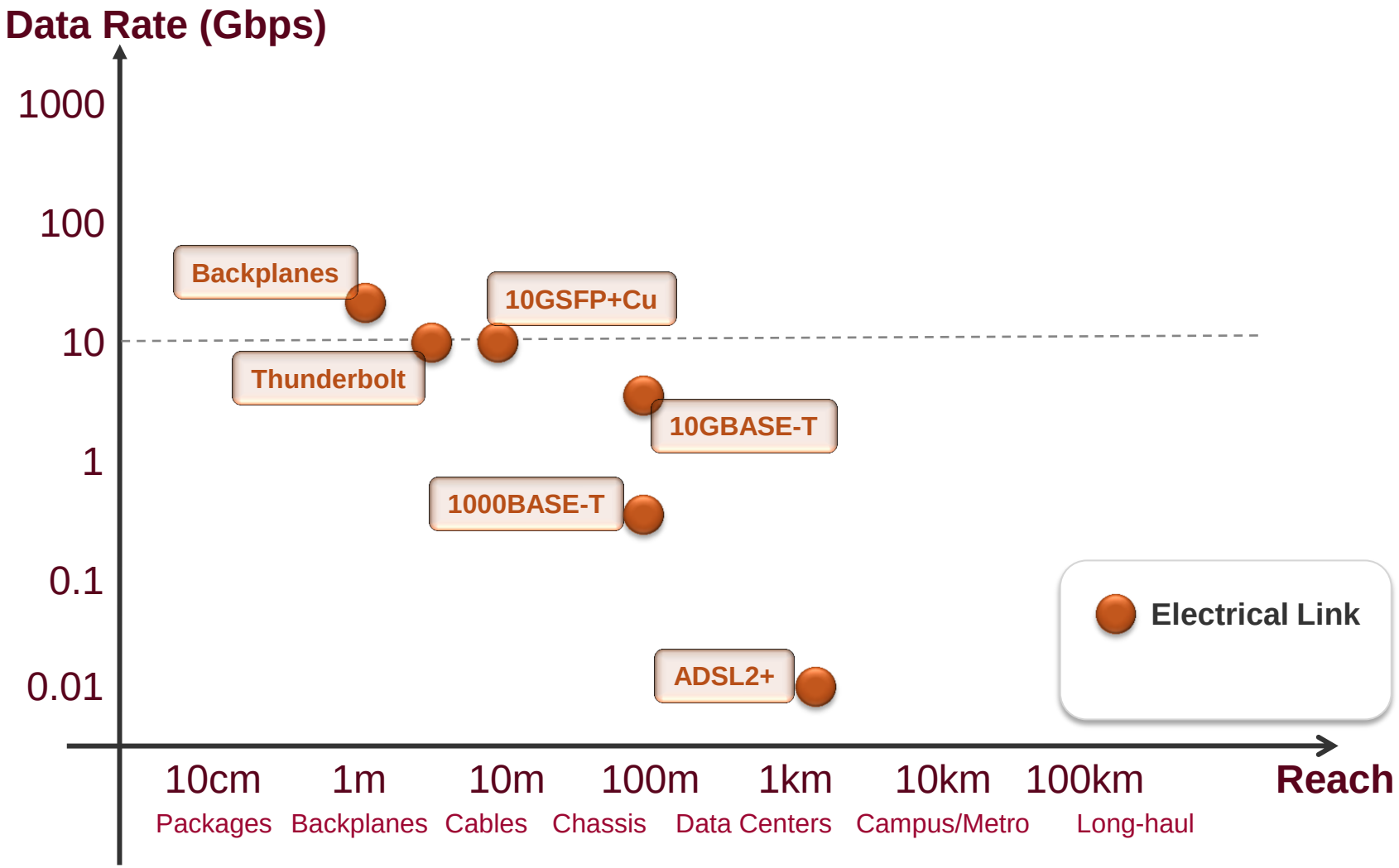
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Overview

1. Electrical vs. Optical Backplanes
2. Optical vs. Optical Backplanes
3. Chip Stacking: a Means to an End

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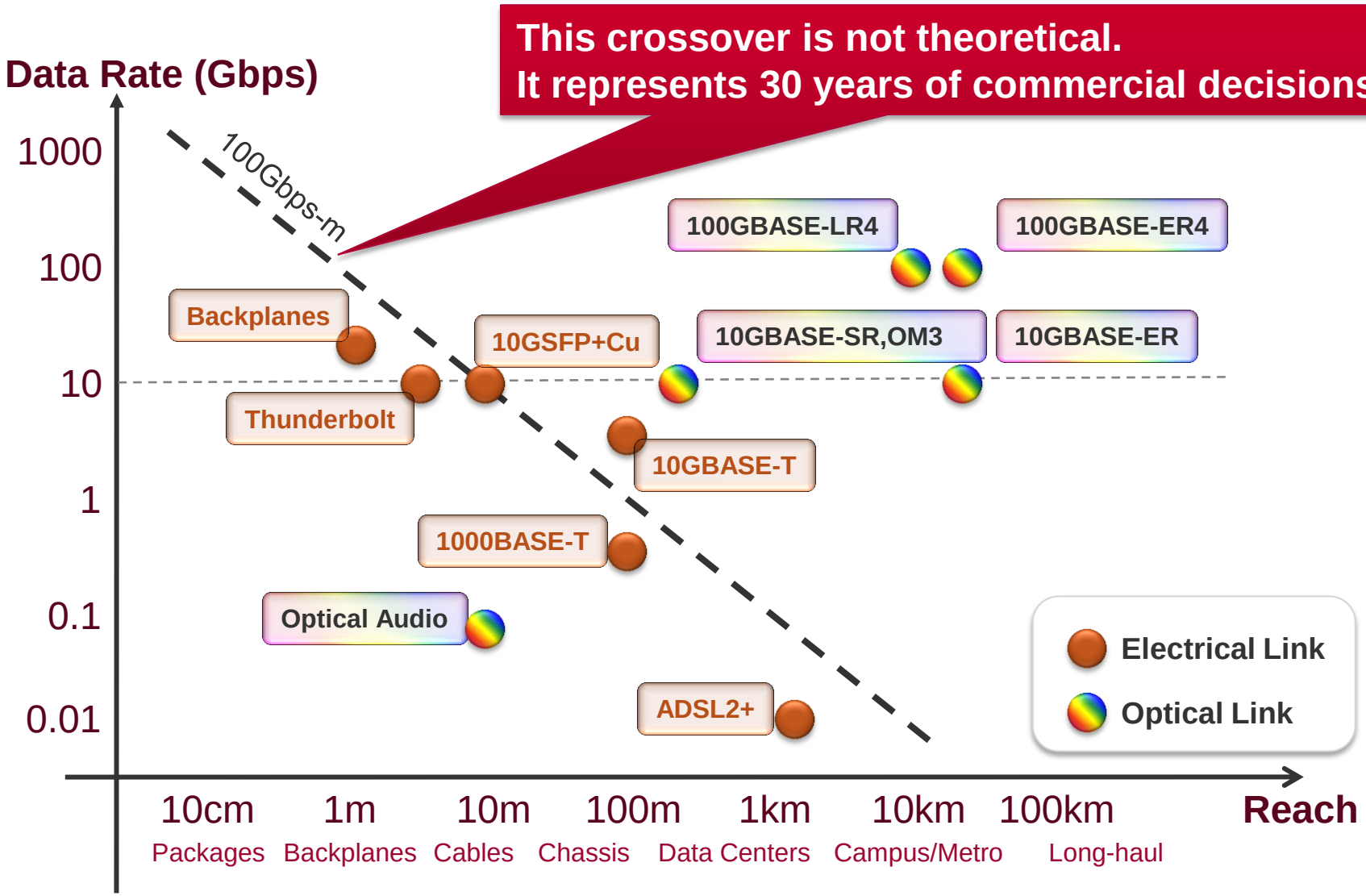
100Gbps-m Electrical-to-Optical Crossover



•Data points from author. Dotted line from Krishnamoorthy, *et al*., "Progress in Low-Power Switched Optical Interconnects," *IEEE J. Selected Topics in Quantum Electronics*, vol. 17, no. 2, 2011.
•1Gbps over 4 copper wire pairs bidirectionally, effectively 0.5Gbps for each wire pair over a maximum distance of 100m (1000GBASE-T spec limit)
•Dong Kam, *et al*., "Is 25Gb/s On-Board Signaling Viable?", IEEE Trans. Adv. Packaging, vol. 32, no. 2, pp 328-344, May 2009.

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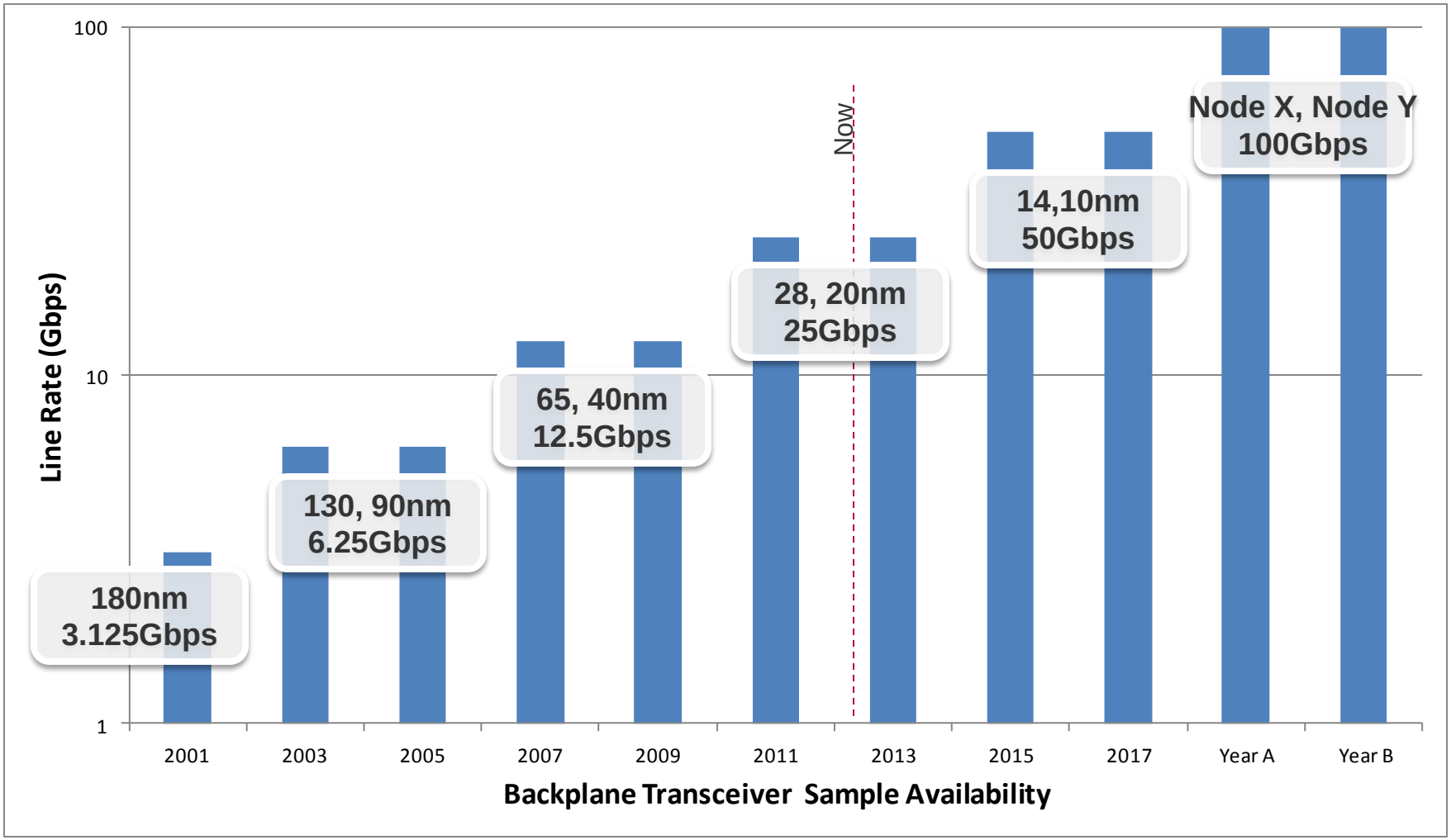
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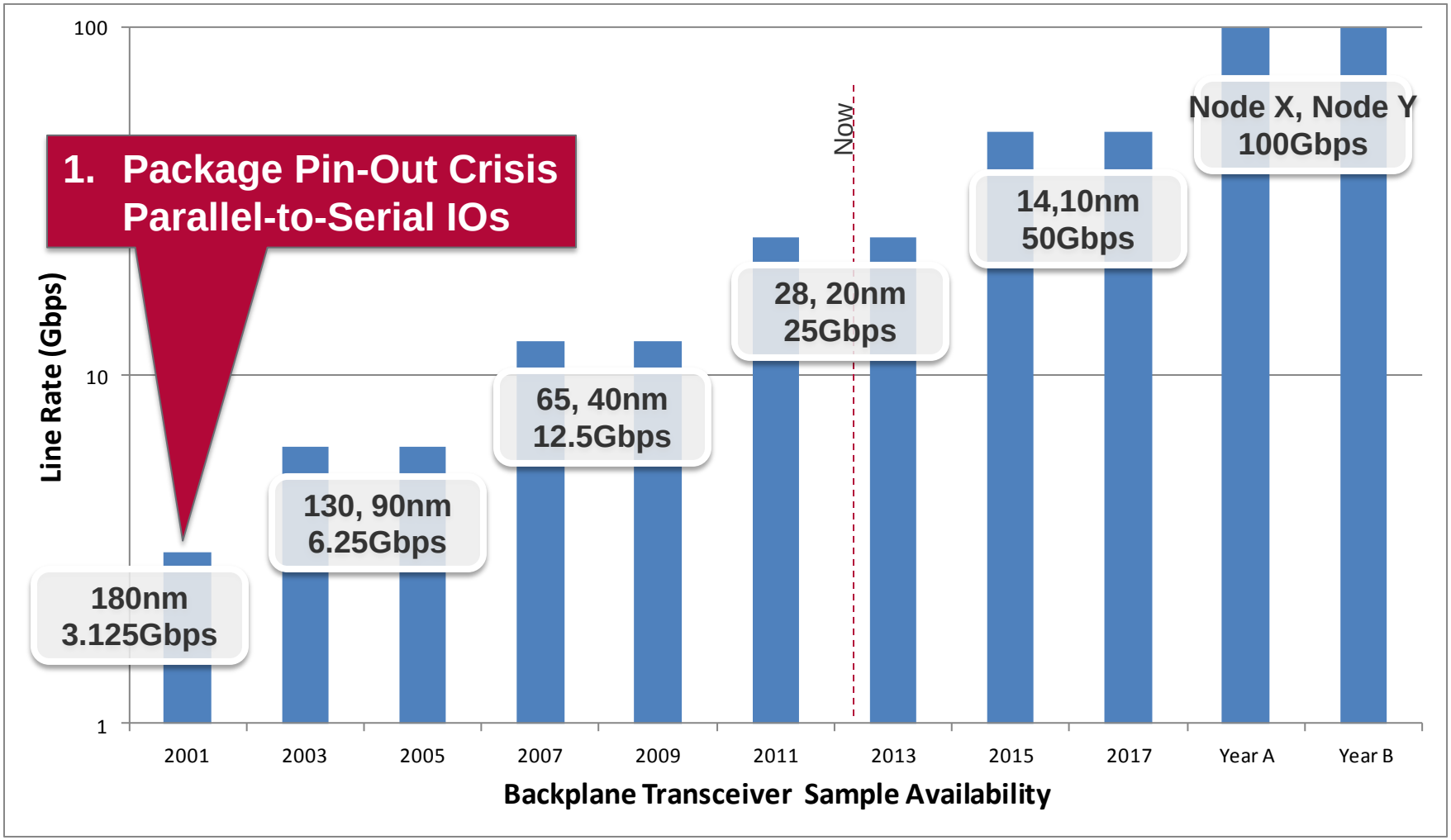
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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes



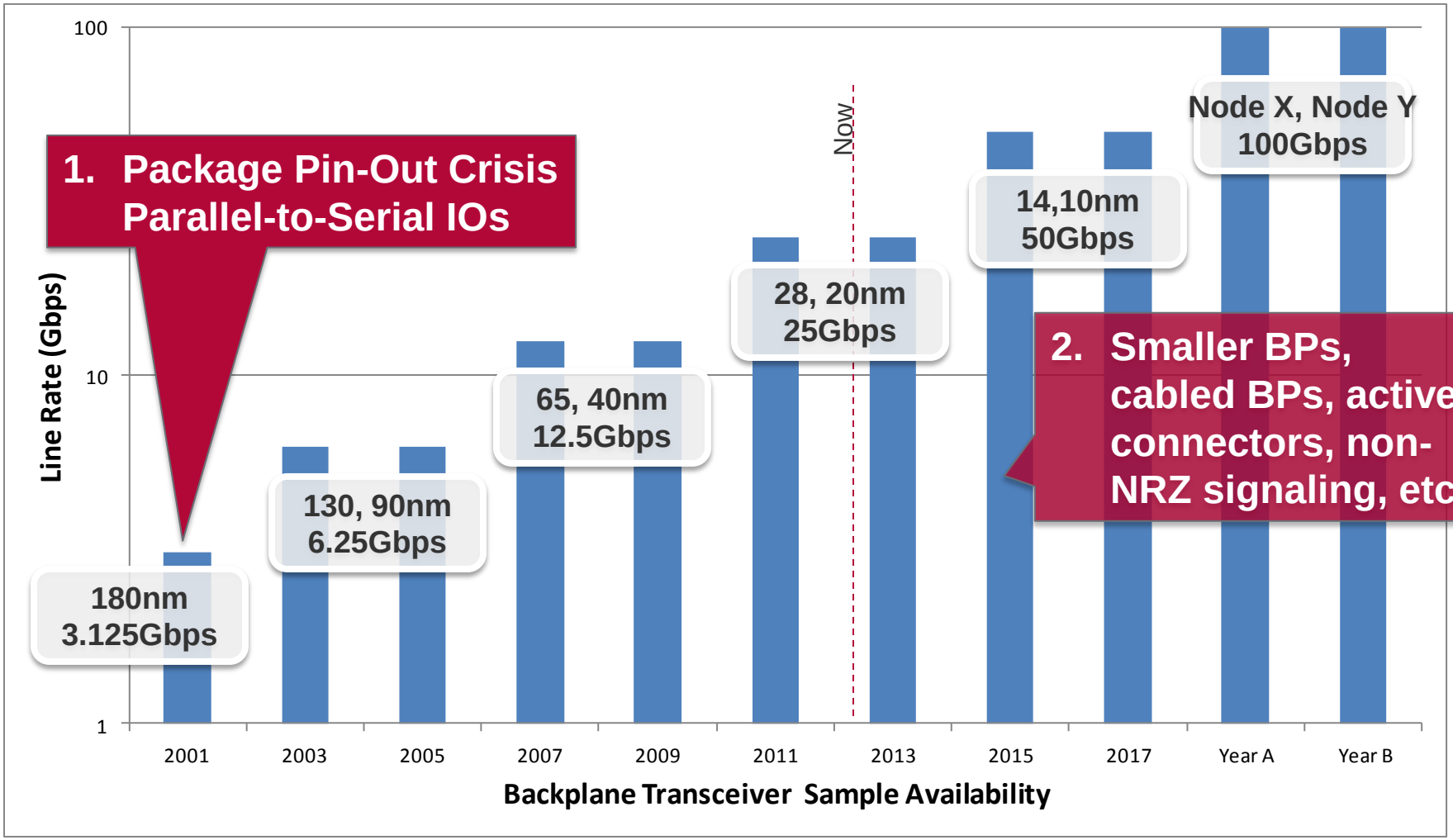
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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes



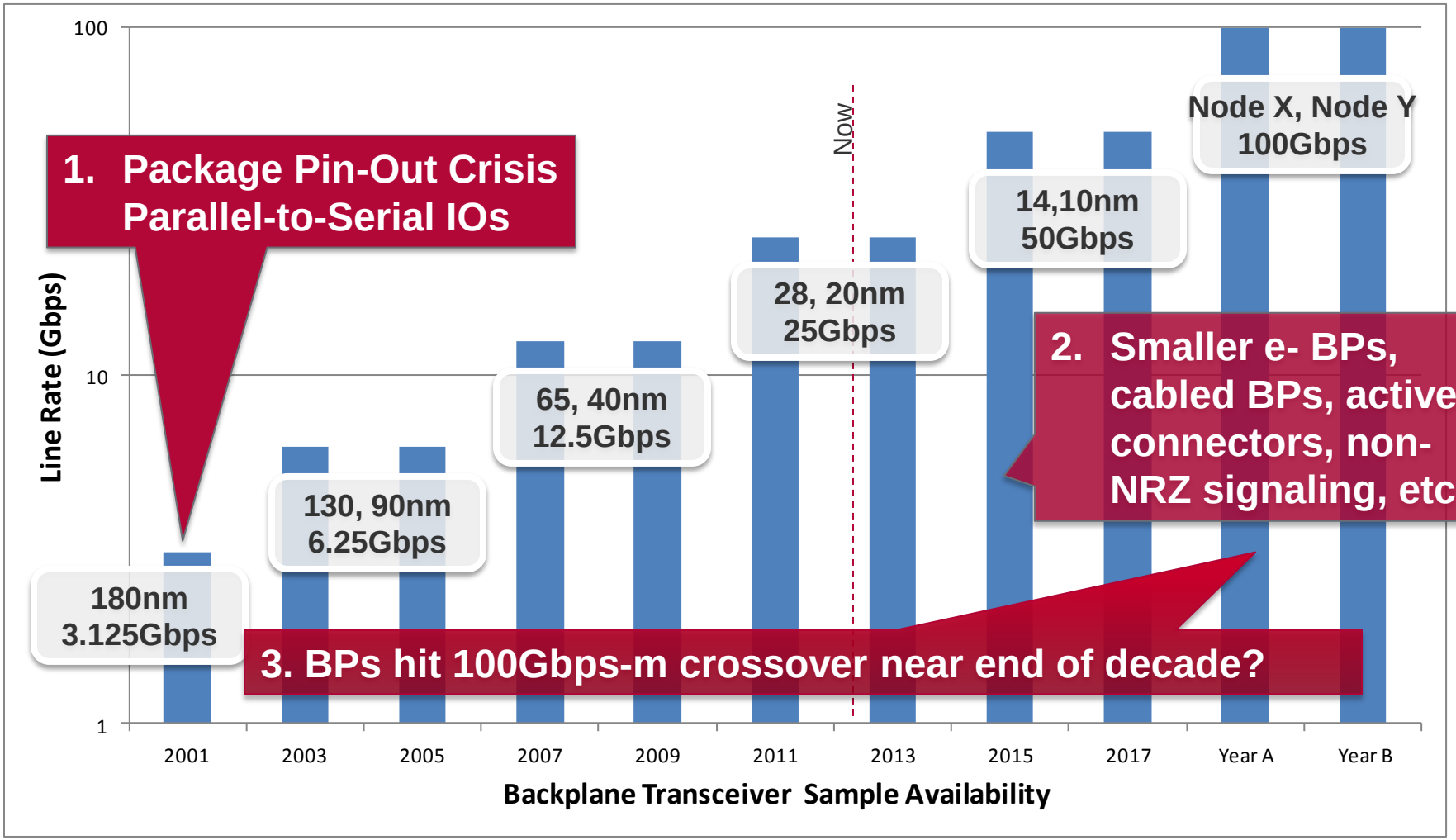
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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes



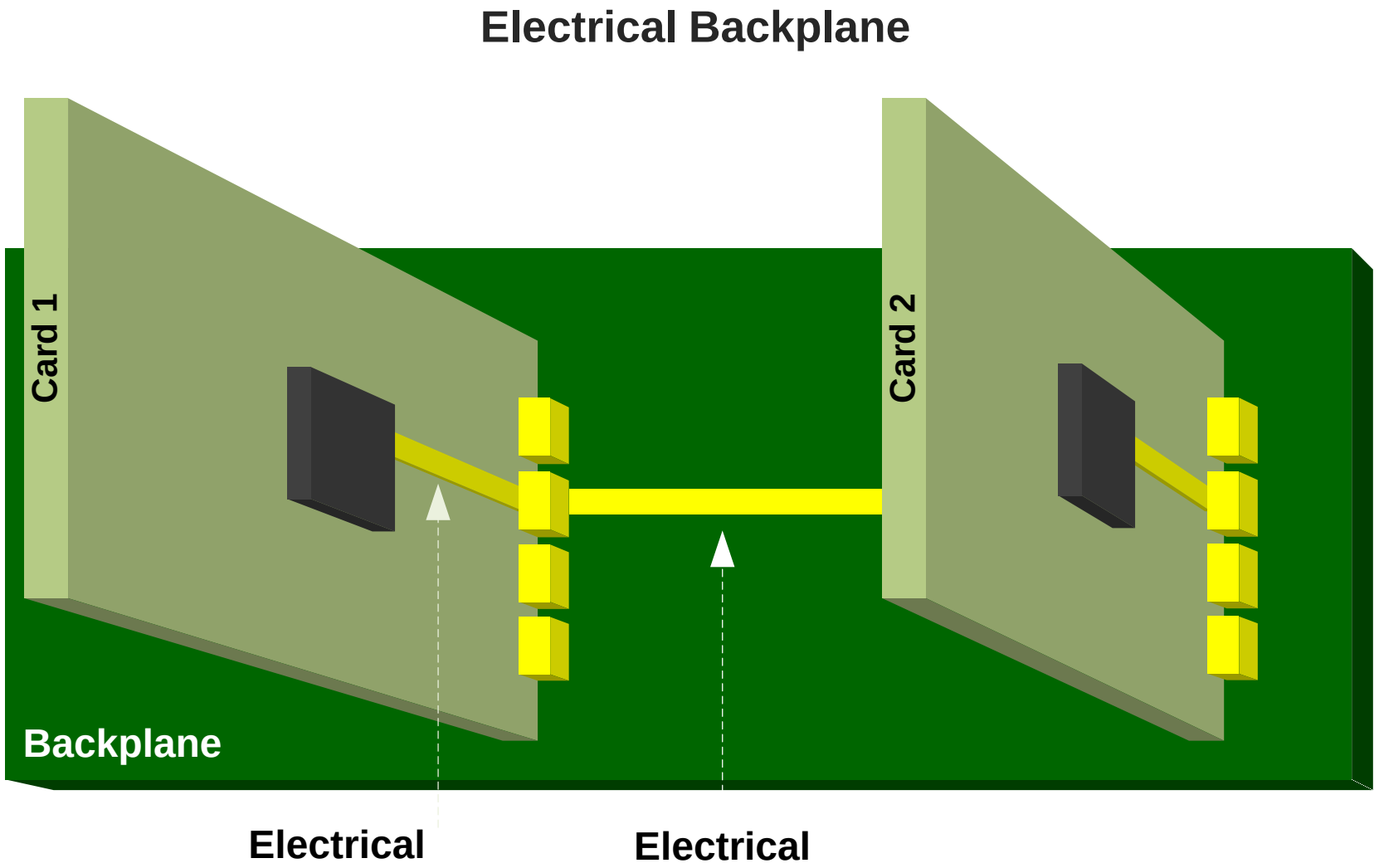
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The Industry Has Managed to Double Backplane Line Rates Every Two Nodes



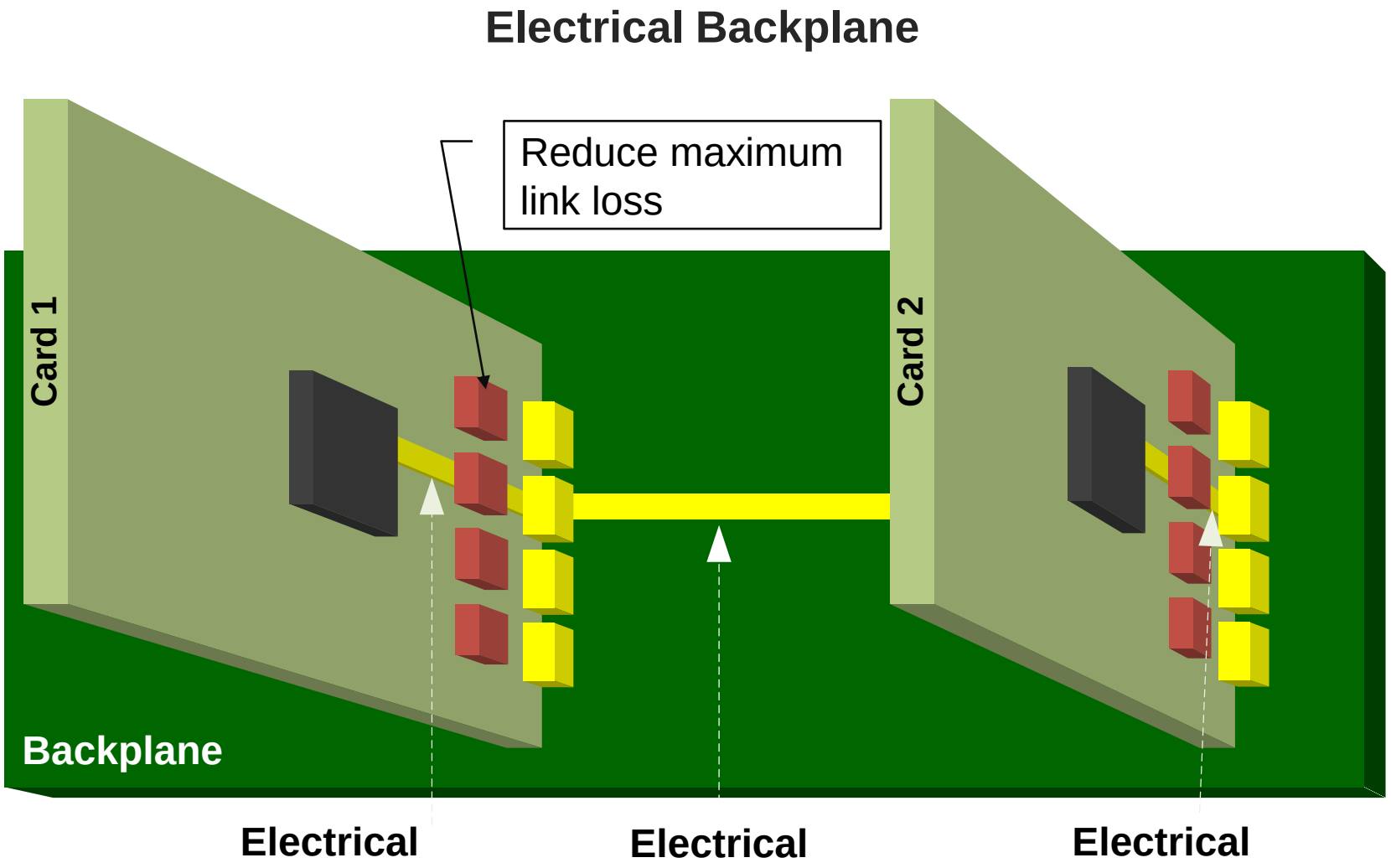
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Electrical vs. Optical Backplanes



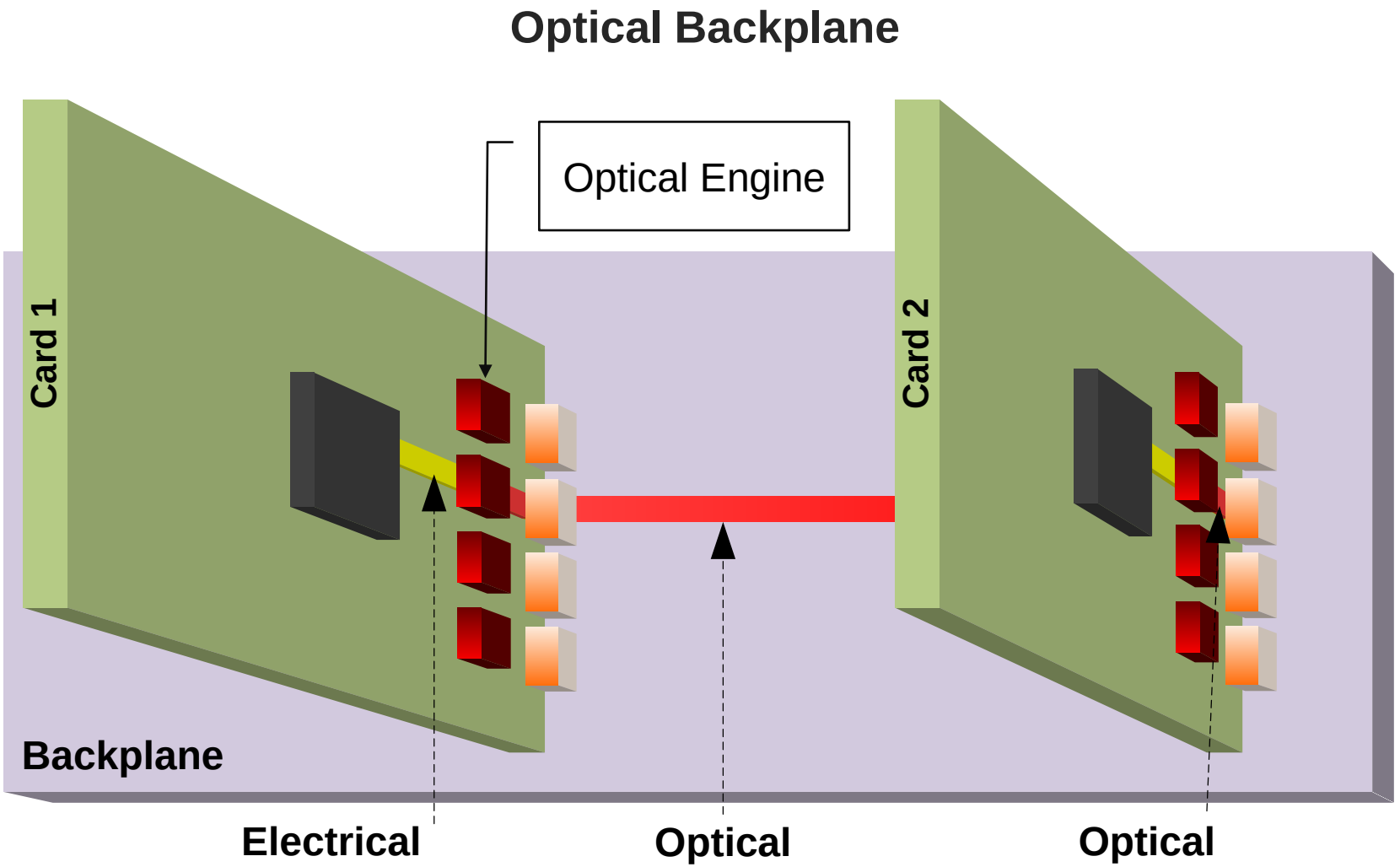
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Electrical vs. Optical Backplanes



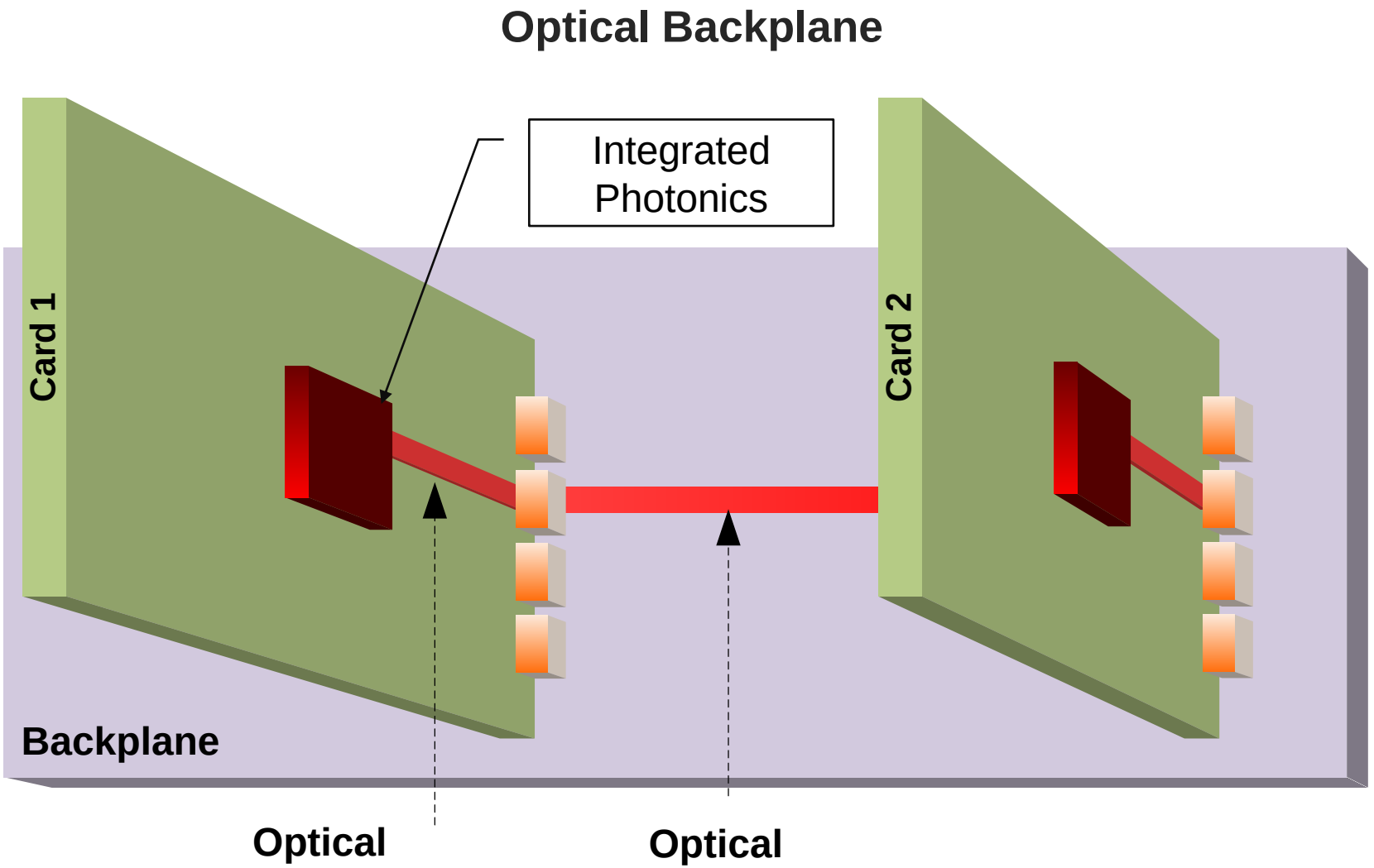
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Electrical vs. Optical Backplanes



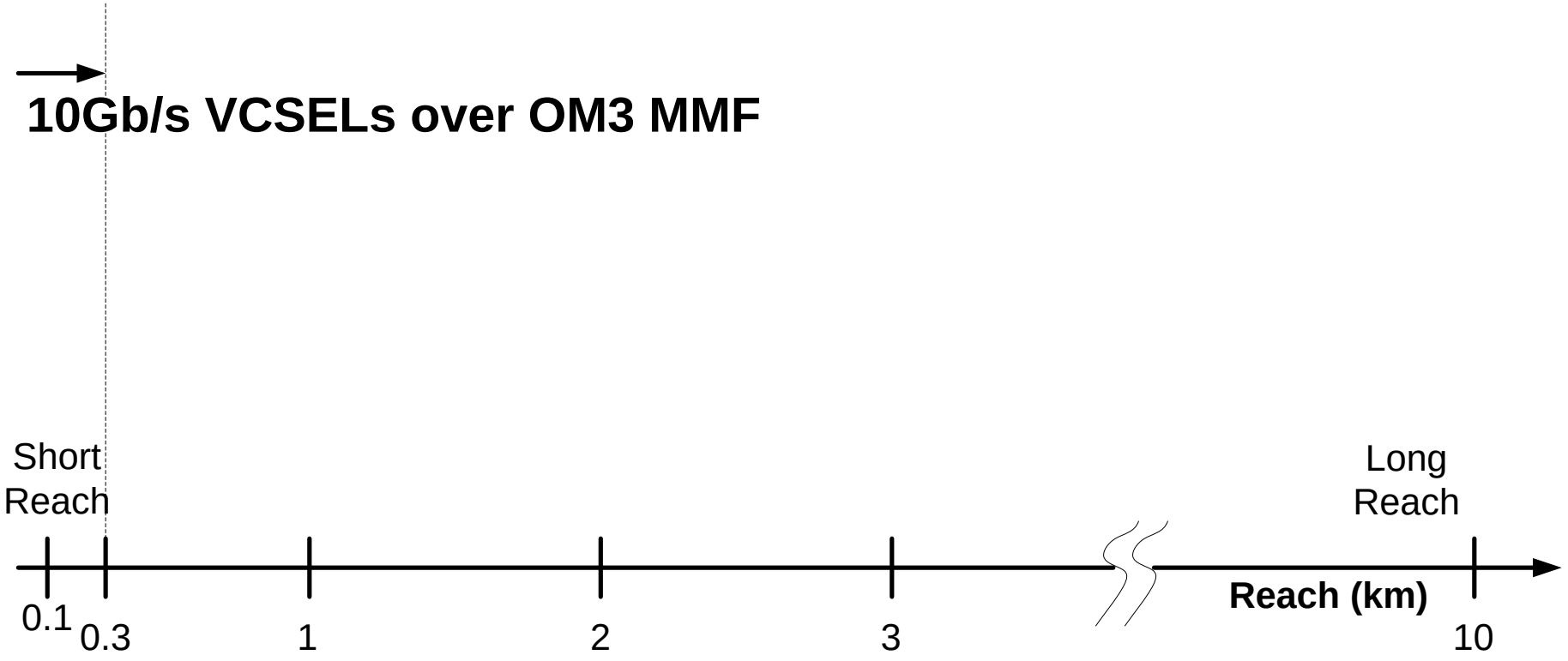
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Electrical vs. Optical Backplanes



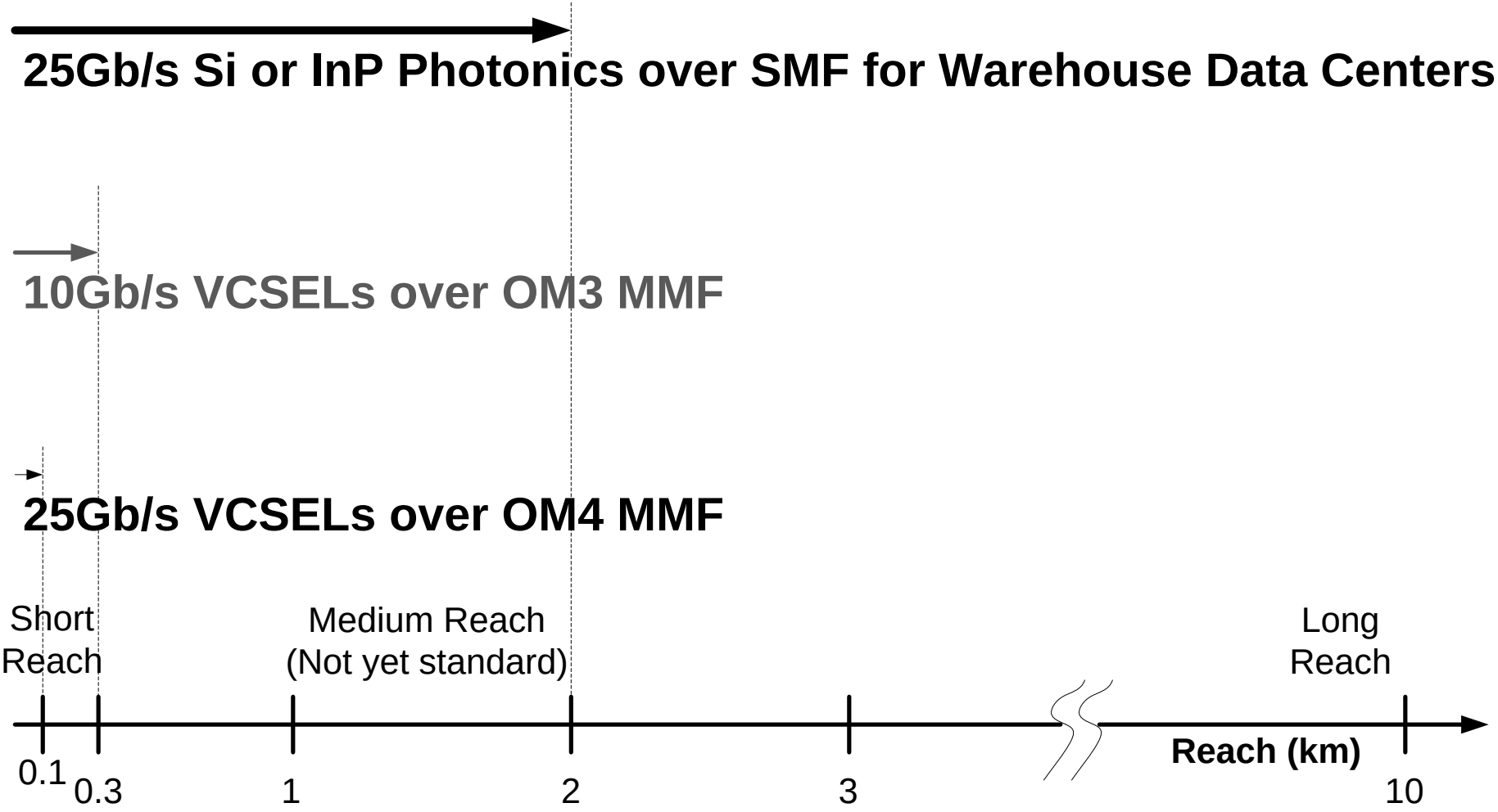
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Optical vs. Optical Backplanes (MMF vs. SMF)
VCSELs: the Incumbent at 10 Gb/s



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Optical vs. Optical Backplanes
Challengers at 25 Gb/s

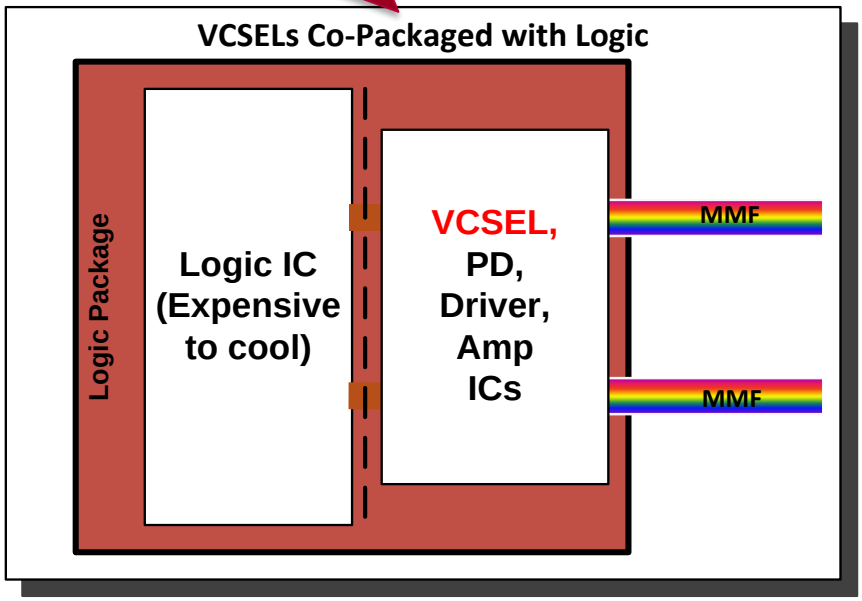


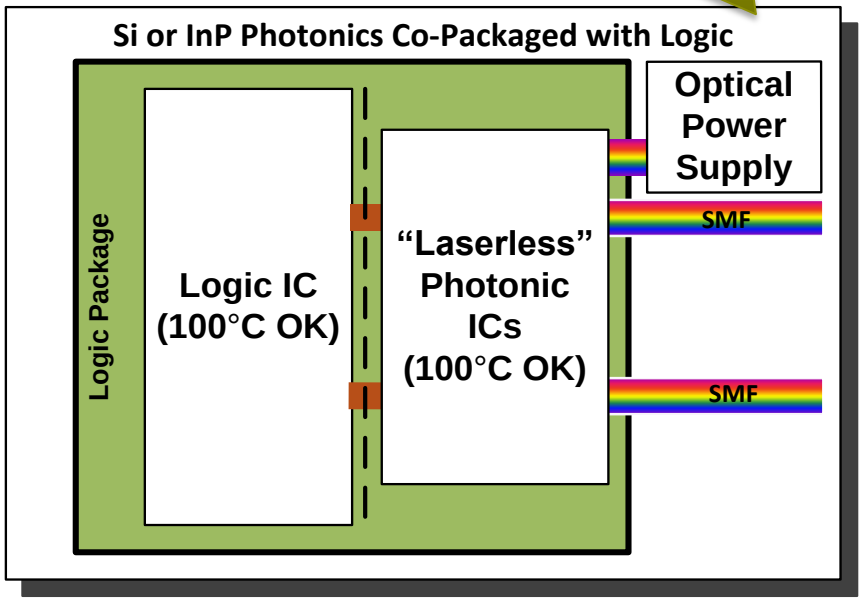
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Optical vs. Optical Backplanes
Options in Stacked Photonics

VCSELs: Laser is Thermal Bottleneck
70°C 850nm MMF to 90°C 1550nm SMF?

Off-Package Optical Power Supply
Evict thermal bottleneck (laser) from package.



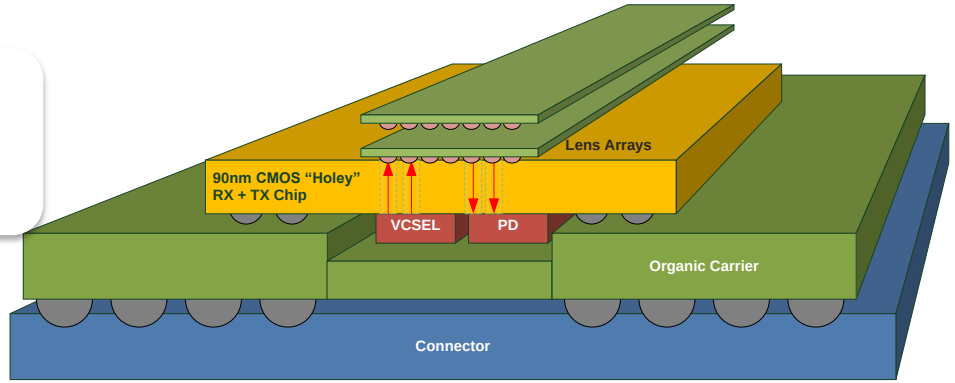


Which technology will scale better?

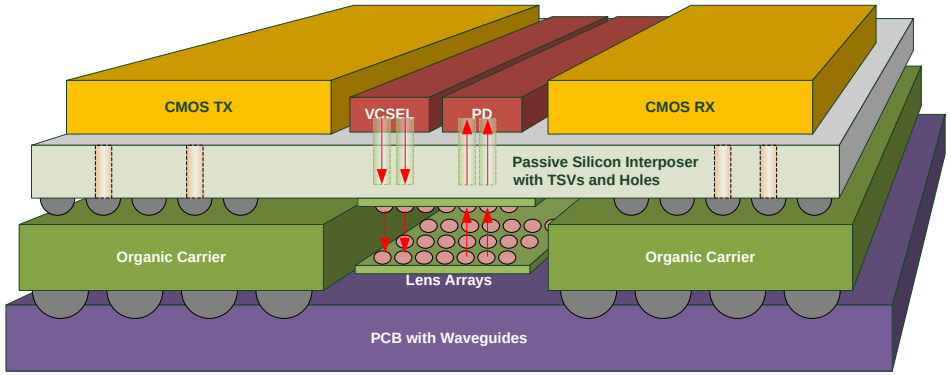
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Stacking Photonics
Who faces up and who faces down?

- **Photonics up for fiber attach**
- **Electronics down and with optical vias (holes)**



- **Photonics down for PWB**
- **Electronics down**
- **Si interposer with holes**

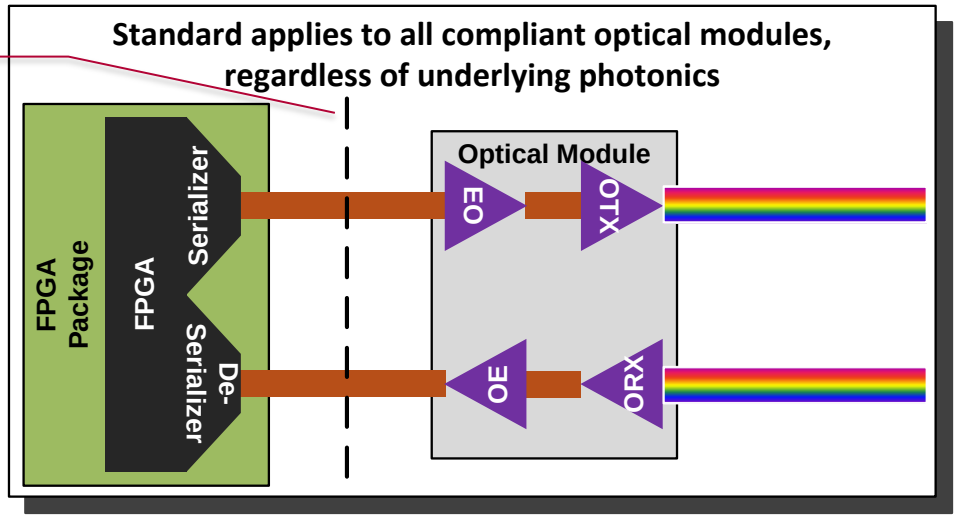


F. Doany, et. al., "Dense 24 TX + 24 RX Fiber-Coupled Optical Module Based on a Holey CMOS Transceiver IC," *60th Electronic Components and Technology Conference,* pp. 248-255, 2010.
F. Doany, et. al., "300-Gb/s 24-Channel Bidirectional Si Carrier Transceiver Optochip for Board-Level Interconnects," *58th Electronic Components and Technology Conference*, pp. 238-243, 2008.
Diagrams redrawn by Xilinx based on papers.

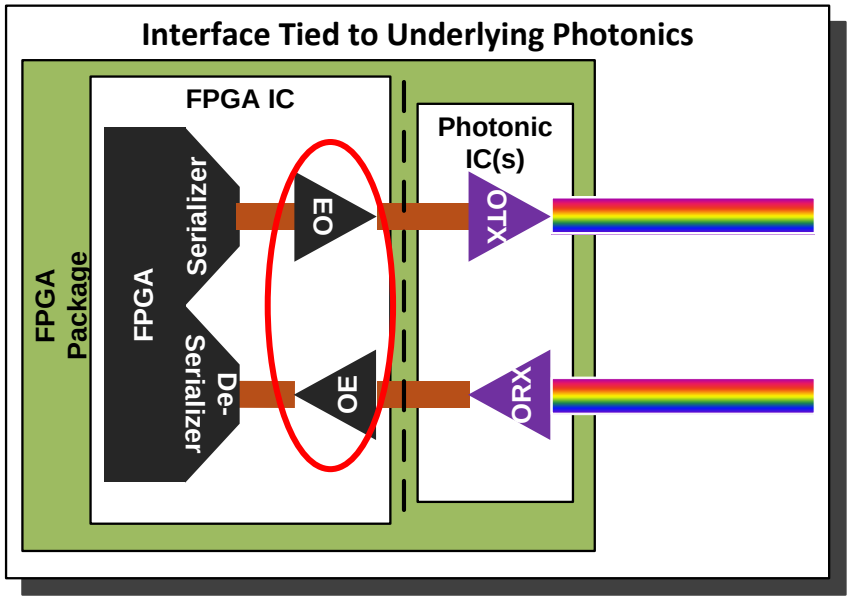
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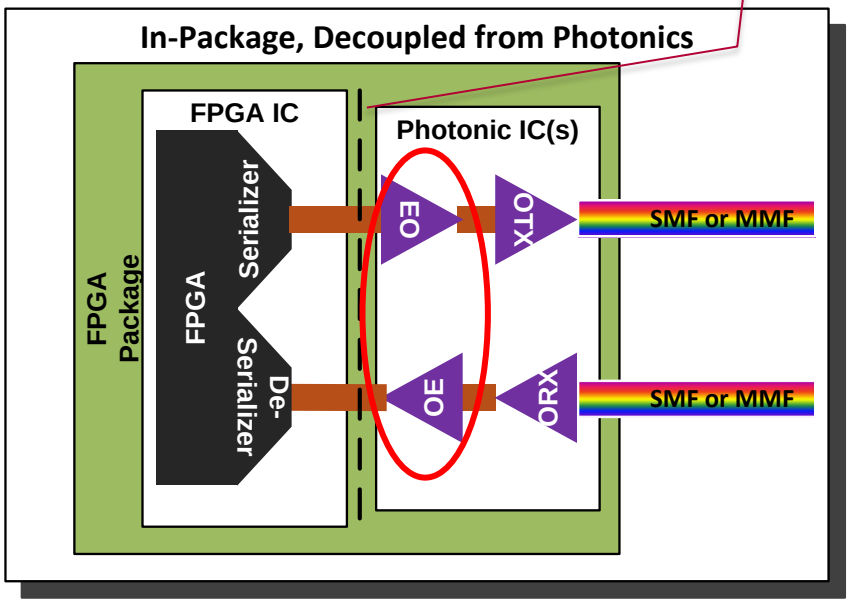
Integrated-Photonics Interface Standards

Example Today: CEI-28G-VSR



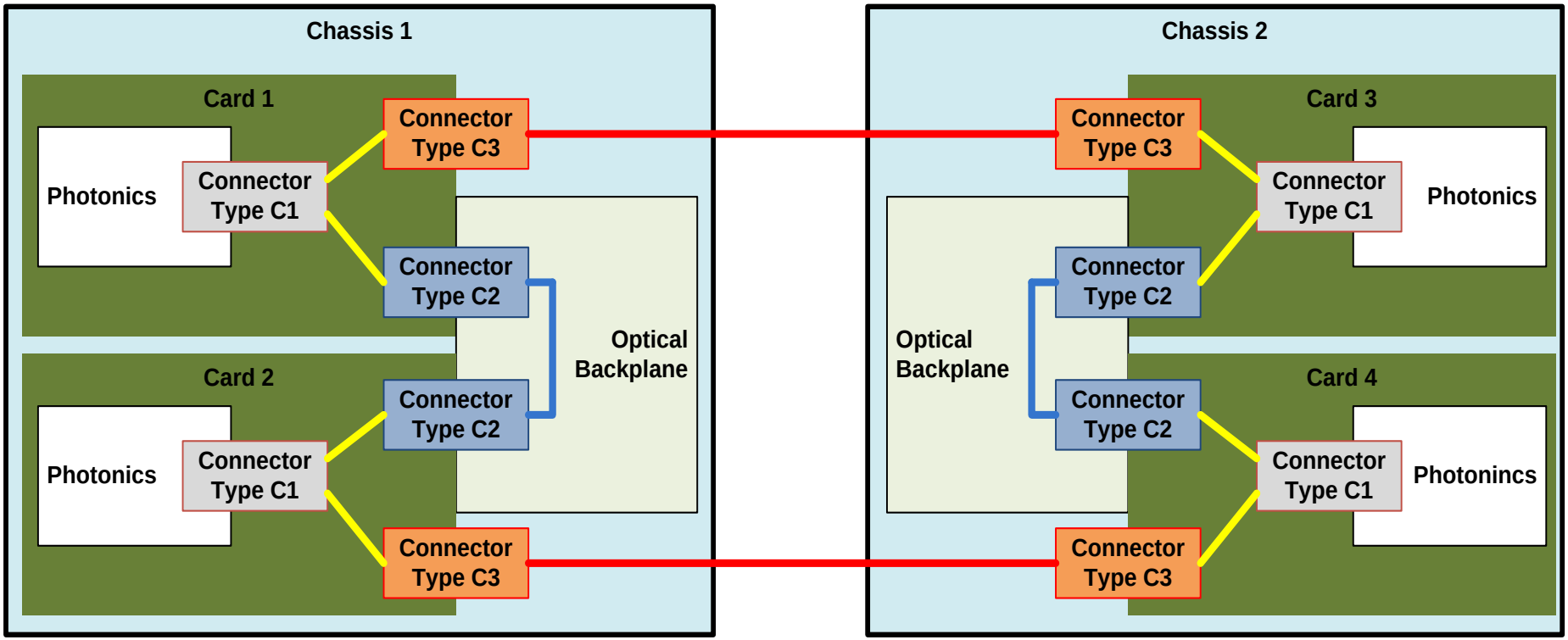
Common electrical inter-IC signaling standard





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What Happens Outside the Chip Matters



Link loss at connectors: Distance-Cost Trade-offs

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Opto-Electronics Supply Chain Needed

Xilinx Stacked-Silicon Supply Chain

FPGA, Interposer, & Package Design
XILINX

28nm FPGA & Interposer
tsmc

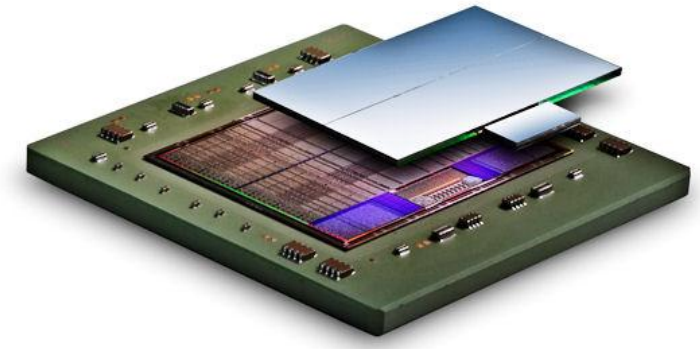
Package Substrate
IBIDEN
KYOCERA

µBump, Die separation
CoC/CoWoS, & Assembly
Amkor Technology
tsmc

Final Test of Packaged Part
XILINX

Opto-Electronics Design
[Names Here]

Opto-Electronics OSAT
[Names Here]



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Summary

1. **Electrical vs. Optical Backplanes**
 Mainstream backplanes to reach crossover near end of decade

2. **Optical vs. Optical Backplanes**
 Choice of VCSELs, InP, and Si Photonics impacts costs & scalability

3. **Chip-stacking is just a means to an end**
 Electrical-to-optical migration: focus on systems and supply chain

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AMD – Bryan Black, Senior Fellow

Abstract

Since room sized computers, advances in technology have been utilized to increase performance reduce power and shrink form factors. Historically new process and packaging technologies have been at the heart of this evolution of ever increasing performance density. Performance density drives our industry creating new compute form factors and usage models for consumers. Interposer and 3D are emerging as the next generation of technologies that will continue to drive performance density. This talk will discuss how die stacking is required by the industry and outline its primary challenges.

Biography

Bryan Black received his Ph.D. from Carnegie Mellon. With over 20 years of experience Black has had the honor of working at Motorola, Intel, and AMD. He has done a little of everything from devices to circuits to microarchitecture to test to packaging. Black is currently a Senior AMD Fellow and runs the AMD die stacking program.

Amkor – ChoonHeung Lee, Corporate VP

Abstract

“Process Integration and Challenges in 2.5D and 3D TSV Assembly”
Small productions in FPGA and Power amplifier applications show that the TSV technology is close to reality even though the supply chain of this technology is still in question. In my context, starting off TSV making in Si at the foundries, MEOL, BEOL and Assembly processes at the OSATs are passed through to be a product. In this talk the processes for MEOL, BEOL and Assembly will be outlined with the process challenges surfaced out. In addition, some issues related to infrastructure building including capacity will be discussed.

Biography

- July 2012 - present : Head of Product Group
- Jan 2010 – present : CTO for RnD and Process/Equipment Engineering
- Feb 1996 – Dec 2009 : Team managers and Head of RnD
- Aug 1986 – Jan 1993 : MS and PhD at Case Western Reserve University
- Mar 1977 – Aug 1985 : BS and MS at Korea University, Marine Corp.

Qualcomm – Riko Radojcic, Director

Abstract

An overview of the principal challenges in the design of various types of 3D stacks is presented with the focus on Memory-on-Logic and Logic-on-Logic class of solutions. A description of the key components of a design flow - PathFinding, TechTuning and Design Authoring - selected to address these challenges is described, and a snap shot of the current status of these solutions is discussed.

Biography

Riko Radojcic is a Director of Engineering at Qualcomm CDMA Technologies, and a leader of various Design-for-Technology initiatives; including Design-for-3D, Design-for-Thermal, Design-for-Manufacturability & Variability, Si-Package CoDesign, etc, and involving methodologies at polygon, circuit, logic, and/or system design levels.

Radojcic has more than thirty year's experience in the semiconductor industry, specializing in the integration of process, design and EDA considerations, and design-for-Si solutions. Before joining Qualcomm, he was a consultant to semiconductor and EDA companies providing engineering and business development services focused on process-design integration. He was a director of business development and marketing for DFM Solutions at PDF Solutions, and a Business Manager and an Architect with Tality and Cadence, specializing in design technology integration and process characterization and modeling.

Radojcic has held a series of managerial and engineering positions with Unisys and Burroughs, in device engineering, failure analyses and reliability engineering areas. He began his career as a process engineer with Ferranti Electronics, UK.

Radojcic received his BSc and PhD degrees from University of Salford, UK.

UMC – Remi Yu, Director Marketing

Abstract

"Foundry TSV Enablement For 2.5D/3D Chip Stacking"
For 2.5D/3D chip stacking applications, foundry has fully demonstrated fine-pitch high density TSV/RDL, leveraging the single/dual damascene Cu processes of advanced CMOS logic fab. This presentation reviews the critical steps of foundry TSV process, test results, applications and related ecosystem work models.

Biography



Remi Yu received the B.S. degree in electrophysics from National Chiao Tung University, Hsinchu, Taiwan in 1989. He is currently deputy director of corporate marketing at United Microelectronics Corporation, with focus on 3D IC and ecosystem marketing. Since joining UMC in 2004, he has worked on the foundry's intellectual property marketing and customer design support. He became a member of the foundry's 3D IC program team starting mid-2011 and has been working on UMC's Open Ecosystem Initiative since. He worked at Macronix International Co., Ltd. prior to joining UMC.

Xilinx – Liam Madden, Corporate VP

Biography



Liam Madden is corporate vice president of FPGA Development and Silicon Technology at Xilinx. He has responsibility for FPGA design, Advanced Packaging (including Stacked Silicon Interconnect) and Foundry Technology. Madden joined Xilinx in 2008, bringing more than 25 years experience in a range of design and technology leadership positions with Digital Equipment Corp., MIPS Technologies, Inc., Microsoft Corp. (XBOX Division), and AMD.

Madden earned a BE from the University College Dublin and a MEng from Cornell University. He holds five patents in the area of technology and circuit design.

Xilinx - Shankar Lakka, Director Integration

Abstract

Xilinx's Stacked Silicon Interconnect (SSI) technology is used to connect multiple FPGAs or other IP die on a single Silicon Interposer. This presentation gives an overview of 3D IC-SSI Technology and Engineering challenges faced during the development of the 3D-IC products. Areas that will be covered are Timing, Physical and Electrical Verification, as well as Signal Integrity.

Biography

Shankar Lakka is the Director of IC Design for full chip FPGA Integration group at Xilinx Inc San Jose. He has been at Xilinx for over 16 years. Shankar has recently led the design and full chip Integration of Xilinx SSI devices. He holds 14 US Patents.

Xilinx - Ephrem Wu, Sr. Director

Abstract

This talk presents a view of when optical interconnects will be prevalent in communications backplanes. It outlines design and supply-chain considerations for 3D-integrated photonics to play a key role in optical backplanes.

Biography

Ephrem Wu is Senior Director of Advanced Communications at Xilinx. He is responsible for advanced FPGA solutions for wireline and wireless communications infrastructure. He joined Xilinx in 2010 and led the design of the industry’s first heterogeneous FPGA. From 2000-2010, Ephrem was with Velio Communications and LSI (which acquired Velio in 2004), leading the definition and development of packet switches and network processors. Prior to Velio, he held various ASIC, circuit, and software design positions at SGI, Hewlett-Packard, Panasonic, and AT&T.

Ephrem earned a BSE degree from Princeton University and an MS degree at the University of California, Berkeley. Both degrees are in EE with an emphasis on computer-aided design. He holds nine patents in switch architecture and circuit design.

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